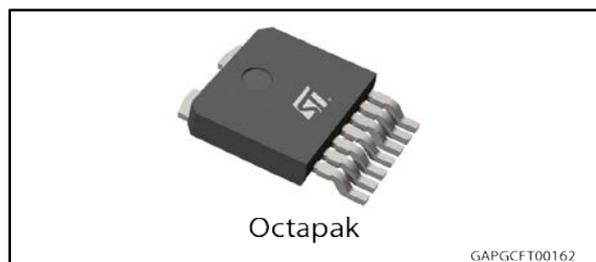


High-side driver with CurrentSense analog feedback for automotive applications

Datasheet - target specification



Features

Max transient supply voltage	V_{CC}	40 V
Operating voltage range	V_{CC}	4 to 28 V
Typ. on-state resistance (per Ch)	R_{ON}	4 m Ω
Current limitation (typ)	I_{LIMH}	112 A
Stand-by current (max)	I_{STBY}	0.5 μ A

- Automotive qualified
- General
 - Single channel smart high-side driver with CurrentSense analog feedback
 - Very low standby current
 - Compatible with 3.0 V and 5 V CMOS outputs
- Diagnostic functions
 - Overload and short to ground (power limitation) indication
 - Thermal shutdown indication
 - OFF-state open-load detection
 - Output short to V_{CC} detection
 - Sense enable/disable
- Protections
 - Undervoltage shutdown
 - Overvoltage clamp
 - Load current limitation

- Self limiting of fast thermal transients
- Loss of ground and loss of V_{CC}
- Reverse battery
- Electrostatic discharge protection

Applications

- All types of Automotive resistive, inductive and capacitive loads
- Specially intended for Automotive Headlamps

Description

The device is a single channel high-side driver manufactured using ST proprietary VIPower® technology and housed in the Octapak package. The device is designed to drive 12 V automotive grounded loads through a 3 V and 5 V CMOS-compatible interface, providing protection and diagnostics.

The device integrates advanced protective functions such as load current limitation, overload active management by power limitation and overtemperature shutdown.

A sense enable pin allows OFF-state diagnosis to be disabled during the module low-power mode as well as external sense resistor sharing among similar devices.

Table 1: Device summary

Package	Order codes
	Tape and reel
Octapak	VN7004CHTR

Contents

1	Block diagram and pin description	5
2	Electrical specification.....	7
2.1	Absolute maximum ratings.....	7
2.2	Thermal data.....	8
2.3	Electrical characteristics.....	8
3	Protections.....	15
3.1	Power limitation.....	15
3.2	Thermal shutdown.....	15
3.3	Current limitation	15
3.4	Negative voltage clamp.....	15
4	Application information	16
4.1	Protection against reverse battery.....	16
4.2	Immunity against transient electrical disturbances.....	17
4.3	MCU I/Os protection.....	17
4.4	CS - analog current sense	18
4.4.1	Principle of CurrentSense signal generation.....	19
4.4.2	Short to VCC and OFF-state open-load detection	21
5	Package and PCB thermal data	23
5.1	Octapak thermal data.....	23
6	Package information	26
6.1	Octapak package information.....	26
6.2	Octapak packing information.....	28
6.3	Octapak marking information	30
7	Revision history	31

List of tables

Table 1: Device summary	1
Table 2: Pin functions	5
Table 3: Suggested connections for unused and not connected pins.....	6
Table 4: Absolute maximum ratings	7
Table 5: Thermal data	8
Table 6: Power section	8
Table 7: Switching.....	9
Table 8: Logic inputs.....	10
Table 9: Protection.....	10
Table 10: CurrentSense.....	11
Table 11: Truth table.....	14
Table 12: ISO 7637-2 - electrical transient conduction along supply line.....	17
Table 13: CurrentSense pin levels in off-state.....	21
Table 14: PCB properties	23
Table 15: Thermal parameters	25
Table 16: Octapak mechanical data	27
Table 17: Reel dimensions	28
Table 18: Document revision history	31

List of figures

Figure 1: Block diagram5
Figure 2: Configuration diagram (top view).....6
Figure 3: Current and voltage conventions.....7
Figure 4: Switching times and Pulse skew13
Figure 5: tDSTKON.....13
Figure 6: Application diagram16
Figure 7: Simplified internal structure16
Figure 8: CurrentSense and diagnostic – block diagram.....18
Figure 9: CurrentSense block diagram19
Figure 10: Analogue HSD – open-load detection in off-state20
Figure 11: Open-load / short to VCC condition.....21
Figure 12: Octapak on two-layers PCB (2s0p to JEDEC JESD 51-5).....23
Figure 13: Octapak on four-layers PCB (2s2p to JEDEC JESD 51-7)23
Figure 14: Rthj-amb vs PCB copper area in open box free air conditions24
Figure 15: Octapak thermal impedance junction ambient single pulse24
Figure 16: Thermal fitting model for Octapak25
Figure 17: Octapak package dimensions26
Figure 18: Octapack reel 13"28
Figure 19: Octapak carrier tape29
Figure 20: Octapak schematic drawing of leader and trailer tape29
Figure 21: Octapak marking information.....30

Figure 2: Configuration diagram (top view)

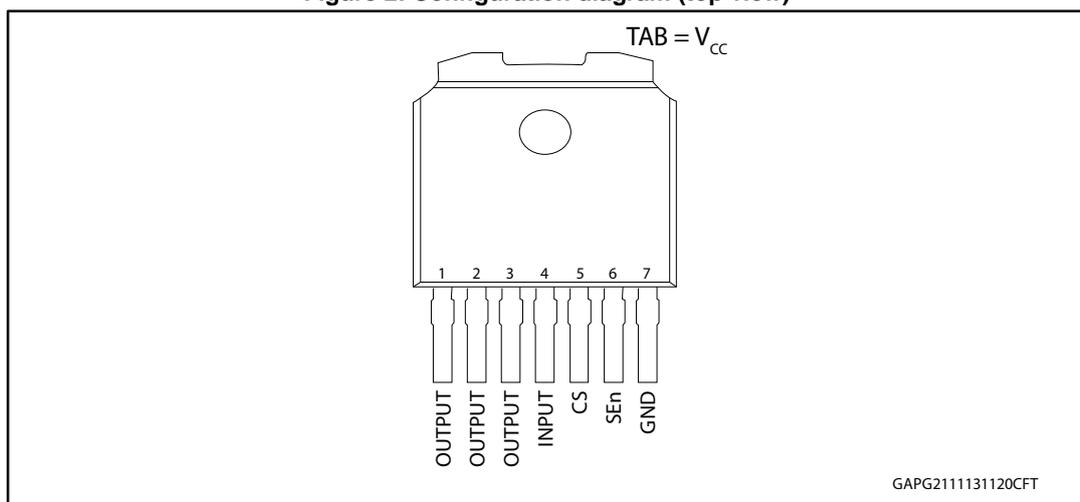


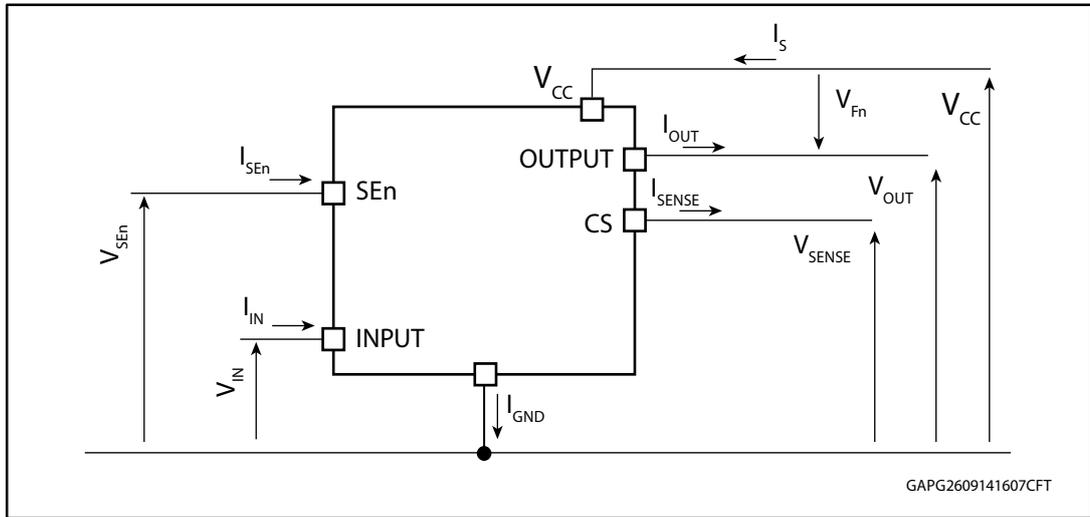
Table 3: Suggested connections for unused and not connected pins

Connection / pin	CurrentSense	N.C.	Output	Input	SEn
Floating	Not allowed	X ⁽¹⁾	X	X	X
To ground	Through 1 k Ω resistor	X	Not allowed	Through 15 k Ω resistor	Through 15 k Ω resistor

Notes:⁽¹⁾X: do not care.

2 Electrical specification

Figure 3: Current and voltage conventions



$V_F = V_{OUT} - V_{CC}$ when $V_{OUT} > V_{CC}$ and INPUT = LOW

2.1 Absolute maximum ratings

Stressing the device above the rating listed in [Table 4: "Absolute maximum ratings"](#) may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to the conditions in table below for extended periods may affect device reliability.

Table 4: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	38	V
V_{CCPK}	Maximum transient supply voltage (ISO7637-2:2004 Pulse 5b level IV clamped to 40 V; $R_L = 4\Omega$)	40	
$-V_{CC}$	Reverse DC supply voltage	16	
$-I_{GND}$	DC reverse ground pin current	200	mA
I_{OUT}	OUTPUT DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	38	
I_{IN}	INPUT DC input current	-1 to 10	mA
I_{SEn}	SEn DC input current		
I_{SENSE}	CS pin DC output current ($V_{GND} = V_{CC}$ and $V_{SENSE} < 0$ V)	10	mA
	CS pin DC output current in reverse ($V_{CC} < 0$ V)	-20	
E_{MAX}	Maximum switching energy (single pulse)	TBD	mJ
	$T_{DEMAG} = 0.4$ ms; $T_{jstart} = 150^\circ\text{C}$		

Symbol	Parameter	Value	Unit
V _{ESD}	Electrostatic discharge (JEDEC 22A-114F)	4000	V
	• INPUT	2000	V
	• CurrentSense	4000	V
	• SEn	4000	V
	• OUTPUT	4000	V
	• V _{CC}	4000	V
V _{ESD}	Charge device model (CDM-AEC-Q100-011)	750	V
T _j	Junction operating temperature	-40 to 150	°C
T _{stg}	Storage temperature	-55 to 150	

2.2 Thermal data

Table 5: Thermal data

Symbol	Parameter	Typ. value	Unit
R _{thj-board}	Thermal resistance junction-board ⁽¹⁾	2.1	°C/W
R _{thj-amb}	Thermal resistance junction-ambient (JEDEC JESD 51-5) ⁽²⁾	57.9	
R _{thj-amb}	Thermal resistance junction-ambient (JEDEC JESD 51-7) ⁽¹⁾	15.4	

Notes:

⁽¹⁾Device mounted on four-layers 2s2p PCB

⁽²⁾Device mounted on two-layers 2s0p PCB with 2 cm² heatsink copper trace

2.3 Electrical characteristics

7 V < V_{CC} < 28 V; -40°C < T_j < 150°C, unless otherwise specified.

All typical values refer to V_{CC} = 13 V; T_j = 25 °C, unless otherwise specified.

Table 6: Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{CC}	Operating supply voltage		4	13	28	V
V _{USD}	Undervoltage shutdown				4	
V _{USDReset}	Undervoltage shutdown reset				5	
V _{USDhyst}	Undervoltage shutdown hysteresis			0.3		
R _{ON}	On-state resistance	I _{OUT} = 15 A; T _j = 25°C		4		mΩ
		I _{OUT} = 15 A; T _j = 150°C			8	
		I _{OUT} = 15 A; V _{CC} = 4 V; T _j = 25°C			6	
R _{ON_Rev}	R _{DS(on)} in reverse battery condition	V _{CC} = -13 V; I _{OUT} = -15 A; T _j = 25°C		4		mΩ
V _{clamp}	Clamp voltage	I _S = 20 mA; T _j = -40°C	38			V
		I _S = 20 mA; 25°C < T _j < 150°C	41	46	52	

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I _{STBY}	Supply current in standby at V _{CC} = 13 V ⁽¹⁾	V _{CC} = 13 V; V _{IN} = V _{OUT} = V _{SEn} = 0 V; T _j = 25°C			0.5	μA
		V _{CC} = 13 V; V _{IN} = V _{OUT} = V _{SEn} = 0 V; T _j = 85°C ⁽²⁾			1.4	μA
		V _{CC} = 13 V; V _{IN} = V _{OUT} = V _{SEn} = 0 V; T _j = 125°C			11	μA
t _{D_STBY}	Standby mode blanking time	V _{CC} = 13 V; V _{IN} = 5 V; V _{SEn} = 0 V; I _{OUT} = 0 A	60	300	550	μs
I _{S(ON)}	Supply current	V _{CC} = 13 V; V _{SEn} = 0 V; V _{IN} = 5 V; I _{OUT} = 0 A		4	6.5	mA
I _{GND(ON)}	Control stage current consumption in ON-state. All channels active.	V _{CC} = 13 V; V _{SEn} = 5 V; V _{IN} = 5 V; I _{OUT} = 15 A			9	mA
I _{L(off)}	Off-state output current at V _{CC} = 13 V	V _{IN} = V _{OUT} = 0 V; V _{CC} = 13 V; T _j = 25°C	0	0.01	0.5	μA
		V _{IN} = V _{OUT} = 0 V; V _{CC} = 13 V; T _j = 125°C	0		11	
V _F	Output - V _{CC} diode voltage	I _{OUT} = -15 A; T _j = 150°C			0.7	V

Notes:

(1)PowerMOS leakage included.

(2)Parameter specified by design; not subject to production test.

Table 7: Switching

V _{CC} = 13 V; -40 °C < T _j < 150 °C, unless otherwise specified						
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{d(on)} ⁽¹⁾	Turn-on delay time at T _j = 25 °C	R _L = 0.87 Ω	10	48	120	μs
t _{d(off)} ⁽¹⁾	Turn-off delay time at T _j = 25 °C		10	58	100	
(dV _{OUT} /dt) _{on} ⁽¹⁾	Turn-on voltage slope at T _j = 25 °C	R _L = 0.87 Ω	0.1	0.3	0.8	V/μs
(dV _{OUT} /dt) _{off} ⁽¹⁾	Turn-off voltage slope at T _j = 25 °C		0.1	0.3	0.8	
W _{ON}	Switching energy losses at turn-on (t _{won})	R _L = 0.87 Ω	—	2	3 ⁽²⁾	mJ
W _{OFF}	Switching energy losses at turn-off (t _{woff})	R _L = 0.87 Ω	—	1.8	3 ⁽²⁾	mJ
t _{SKEW} ⁽¹⁾	Differential Pulse skew (t _{PHL} - t _{PLH})	R _L = 0.87 Ω	-35	15	65	μs

Notes:(1)See [Figure 4: "Switching times and Pulse skew"](#)

(2)Parameter guaranteed by design and characterization; not subject to production test.

Table 8: Logic inputs

7 V < V _{CC} < 28 V; -40 °C < T _j < 150 °C						
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
INPUT characteristics						
V _{IL}	Input low level voltage				0.9	V
I _{IL}	Low level input current	V _{IN} = 0.9 V	1			μA
V _{IH}	Input high level voltage		2.1			V
I _{IH}	High level input current	V _{IN} = 2.1 V			10	μA
V _{I(hyst)}	Input hysteresis voltage		0.2			V
V _{ICL}	Input clamp voltage	I _{IN} = 1 mA	5.3		7.5	V
		I _{IN} = -1 mA		-0.7		
SEn characteristics (7 V < V_{CC} < 18 V)						
V _{SEnL}	Input low level voltage				0.9	V
I _{SEnL}	Low level input current	V _{IN} = 0.9 V	1			μA
V _{SEnH}	Input high level voltage		2.1			V
I _{SEnH}	High level input current	V _{IN} = 2.1 V			10	μA
V _{SEn(hyst)}	Input hysteresis voltage		0.2			V
V _{SEnCL}	Input clamp voltage	I _{IN} = 1 mA	5.3		7.5	V
		I _{IN} = -1 mA		-0.7		

Table 9: Protection

7 V < V _{CC} < 18 V; -40 °C < T _j < 150 °C						
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I _{LIMH} ⁽¹⁾	DC short circuit current	V _{CC} = 13 V	80	112	160	A
		4 V < V _{CC} < 18 V ⁽²⁾			160	
I _{LIML}	Short circuit current during thermal cycling	V _{CC} = 13 V; T _R < T _j < T _{TSD}		33		
T _{TSD}	Shutdown temperature		150	175	200	°C
T _R	Reset temperature ⁽²⁾		T _{RS} + 1	T _{RS} + 7		
T _{RS}	Thermal reset of fault diagnostic indication	V _{SEn} = 5 V	135			
T _{HYST}	Thermal hysteresis (T _{TSD} - T _R) ⁽²⁾			7		
ΔT _{J_SD}	Dynamic temperature	T _j = -40°C; V _{CC} = 13 V		60		K
V _{DEMAG}	Turn-off output voltage clamp	I _{OUT} = 2 A; L = 6 mH; T _j = -40°C	V _{CC} - 38			V
		I _{OUT} = 2 A; L = 6 mH; T _j = 25°C to 150°C	V _{CC} - 41	V _{CC} - 46	V _{CC} - 52	V

Notes:

⁽¹⁾Parameter guaranteed by an indirect test sequence.

⁽²⁾Parameter guaranteed by design and characterization; not subject to production test.

Table 10: CurrentSense

7 V < V _{CC} < 18 V; -40 °C < T _j < 150 °C						
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{SENSE_CL}	CurrentSense clamp voltage	V _{SEN} = 0 V; I _{SENSE} = 1 mA	-17		-12	V
		V _{SEN} = 0 V; I _{SENSE} = -1 mA		7		V
Current Sense characteristics						
K ₁	I _{OUT} /I _{SENSE}	I _{OUT} = 10 A; V _{SENSE} = 4 V; V _{SEN} = 5 V	10040	16720	23400	
dK ₁ /K ₁ ⁽¹⁾⁽²⁾	Current sense ratio drift	I _{OUT} = 10 A; V _{SENSE} = 4 V; V _{SEN} = 5 V	-20		20	%
K ₂	I _{OUT} /I _{SENSE}	I _{OUT} = 15 A; V _{SENSE} = 4 V; V _{SEN} = 5 V	12530	16710	20890	
dK ₂ /K ₂ ⁽¹⁾⁽²⁾	Current sense ratio drift	I _{OUT} = 15 A; V _{SENSE} = 4 V; V _{SEN} = 5 V	-15		15	%
K ₃	I _{OUT} /I _{SENSE}	I _{OUT} = 45 A; V _{SENSE} = 4 V; V _{SEN} = 5 V	14450	16970	18850	
dK ₃ /K ₃ ⁽¹⁾⁽²⁾	Current sense ratio drift	I _{OUT} = 45 A; V _{SENSE} = 4 V; V _{SEN} = 5 V	-10		10	%
I _{SENSE0}	CurrentSense leakage current	CurrentSense disabled: V _{SEN} = 0 V;	0		0.5	μA
		CurrentSense disabled; -1 V < V _{SENSE} < 5 V ⁽²⁾	-0.5		0.5	μA
		CurrentSense enabled: V _{SEN} = 5 V; V _{IN} = 5 V; I _{OUT} = 0 A;	0		100	μA
V _{OUT_CSD} ⁽²⁾	Output voltage for CurrentSense shutdown	V _{SEN} = 5 V; R _{SENSE} = 2.7 kΩ; V _{IN} = 5 V; I _{OUT} = 15 A		5		V
V _{SENSE_SAT}	CurrentSense saturation voltage	V _{CC} = 7 V; R _{SENSE} = 2.7 kΩ; V _{SEN} = 5 V; V _{IN} = 5 V; I _{OUT} = 45 A; T _j = 150°C	5			V
I _{SENSE_SAT} ⁽²⁾	CS saturation current	V _{CC} = 7 V; V _{SENSE} = 4 V; V _{IN} = 5 V; V _{SEN} = 5 V; T _j = 150°C	4			mA
I _{OUT_SAT} ⁽²⁾	Output saturation current	V _{CC} = 7 V; V _{SENSE} = 4 V; V _{IN} = 5 V; V _{SEN} = 5 V; T _j = 150°C	75			A
OFF-state diagnostic						
V _{OL}	OFF-state open-load voltage detection threshold	V _{IN} = 0 V; V _{SEN} = 5 V;	2	3	4	V
I _{L(off2)}	OFF-state output sink current	V _{IN} = 0 V; V _{OUT} = V _{OL} ; T _j = -40°C to 125°C	-100		-15	μA
t _{DSTKON}	OFF-state diagnostic delay time from falling edge of INPUT (see Figure 5: "tDSTKON")	V _{IN} = 5 V to 0 V; V _{SEN} = 5 V; I _{OUT} = 0 A; V _{OUT} = 4 V	100	350	700	μs

7 V < V _{CC} < 18 V; -40 °C < T _j < 150 °C						
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{D_OL_V}	Settling time for valid OFF-state open load diagnostic indication from rising edge of SEn	V _{IN} = 0 V; V _{OUT} = 4 V; V _{SEn} = 0 V to 5 V			60	µs
t _{D_VOL}	OFF-state diagnostic delay time from rising edge of V _{OUT}	V _{IN} = 0 V; V _{SEn} = 5 V; V _{OUT} = 0 V to 4 V		5	30	µs
Fault diagnostic feedback (see Table 11: "Truth table")						
V _{SENSEH}	CurrentSense output voltage in fault condition	V _{CC} = 13 V; V _{IN} = 0 V; V _{SEn} = 5 V; I _{OUT} = 0 A; V _{OUT} = 4 V; R _{SENSE} = 1 kΩ	5		6.6	V
I _{SENSEH}	CurrentSense output current in fault condition	V _{CC} = 13 V; V _{SENSE} = 5 V	7	20	30	mA
CurrentSense timings (current sense mode)⁽³⁾						
t _{DSSENSE1H}	Current sense settling time from rising edge of SEn	V _{IN} = 5 V; V _{SEn} = 0 V to 5 V; R _{SENSE} = 1 kΩ; R _L = 0.87 kΩ			60	µs
t _{DSSENSE1L}	Current sense disable delay time from falling edge of SEn	V _{IN} = 5 V; V _{SEn} = 5 V to 0 V; R _{SENSE} = 1 kΩ; R _L = 0.87 kΩ		5	20	µs
t _{DSSENSE2H}	Current sense settling time from rising edge of INPUT	V _{IN} = 0 V to 5 V; V _{SEn} = 5 V; R _{SENSE} = 1 kΩ; R _L = 0.87 kΩ		100	300	µs
Δt _{DSSENSE2H}	Current sense settling time from rising edge of I _{OUT} (dynamic response to a step change of I _{OUT})	V _{IN} = 5 V; V _{SEn} = 5 V; R _{SENSE} = 1 kΩ; I _{SENSE} = 90% of I _{SENSEMAX} ; R _L = 0.87 kΩ			200	µs
t _{DSSENSE2L}	Current sense turn-off delay time from falling edge of INPUT	V _{IN} = 5 V to 0 V; V _{SEn} = 5 V; R _{SENSE} = 1 kΩ; R _L = 0.87 kΩ		50	250	µs

Notes:

- (1) All values refer to V_{CC} = 13 V; T_j = 25°C, unless otherwise specified.
- (2) Parameter guaranteed by design and characterization; not subject to production test.
- (3) Transition delay are measured up to ±10% of final conditions.

Figure 4: Switching times and Pulse skew

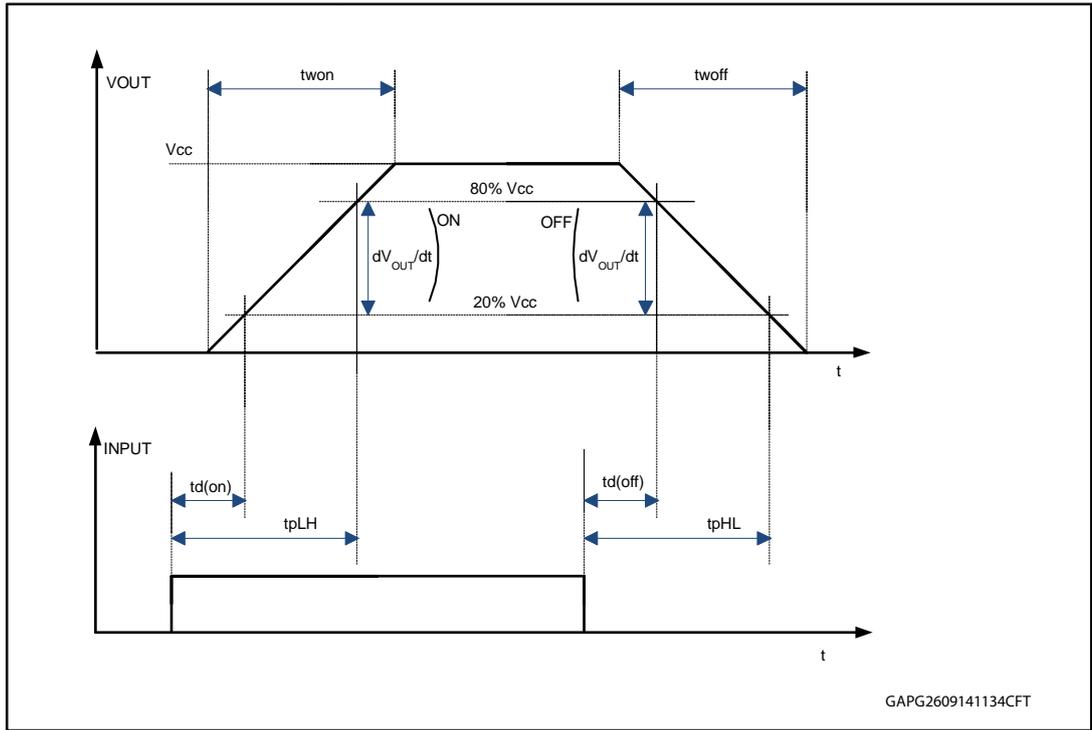


Figure 5: t_{DSTKON}

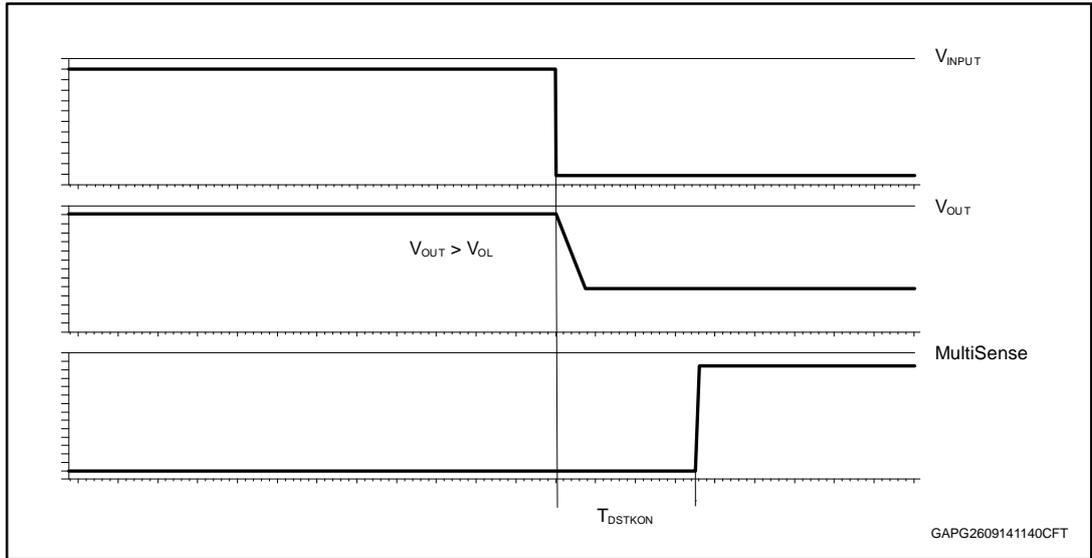


Table 11: Truth table

Mode	Conditions	IN _x	SEn	OUT _x	Current Sense	Comments
Stand by	All logic inputs low	L	L	L	Hi-Z	Low quiescent current consumption
Normal	Nominal load connected; T _j < 150°C	L	H	L	0	
		H	L	H	Hi-Z	
		H	H	H	I _{SENSE} = 1/K * I _{OUT}	
Overload	Overload or short to GND causing: T _j > T _{TSD} or ΔT _j > ΔT _{j,SD}	H	L	H	Hi-Z	Output cycles with temperature hysteresis
		H	H	H	V _{SENSEH}	
Under-voltage	V _{CC} < V _{USD} (falling)	X	X	L L	Hi-Z Hi-Z	Re-start when V _{CC} > V _{USD} + V _{USDhyst} (rising)
OFF-state diagnostics	Short to V _{CC}	L	H	H	V _{SENSEH}	
	Open-load	L	H	H		External pull-up
Negative output voltage	Inductive loads turn-off	L	X	< 0 V	0	

3 Protections

3.1 Power limitation

The basic working principle of this protection consists of an indirect measurement of the junction temperature swing ΔT_j through the direct measurement of the spatial temperature gradient on the device surface in order to automatically shut off the output MOSFET as soon as ΔT_j exceeds the safety level of ΔT_{j_SD} . The protection prevents fast thermal transient effects and, consequently, reduces thermo-mechanical fatigue.

3.2 Thermal shutdown

In case the junction temperature of the device exceeds the maximum allowed threshold (typically 175°C), it automatically switches off and the diagnostic indication is triggered. The device switches on again as soon as its junction temperature drops to T_R .

3.3 Current limitation

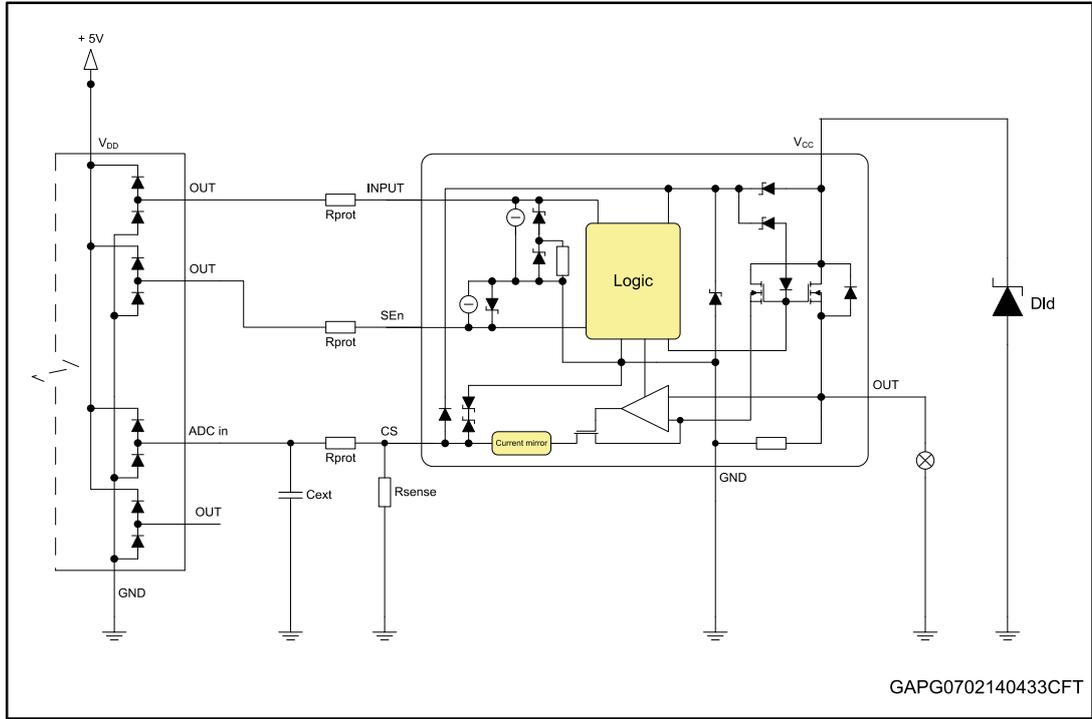
The device is equipped with an output current limiter in order to protect the silicon as well as the other components of the system (e.g. bonding wires, wiring harness, connectors, loads, etc.) from excessive current flow. Consequently, in case of short circuit, overload or during load power-up, the output current is clamped to a safety level, I_{LIMH} , by operating the output power MOSFET in the active region.

3.4 Negative voltage clamp

In case the device drives inductive load, the output voltage reaches negative value during turn off. A negative voltage clamp structure limits the maximum negative voltage to a certain value, V_{DEMAG} , allowing the inductor energy to be dissipated without damaging the device.

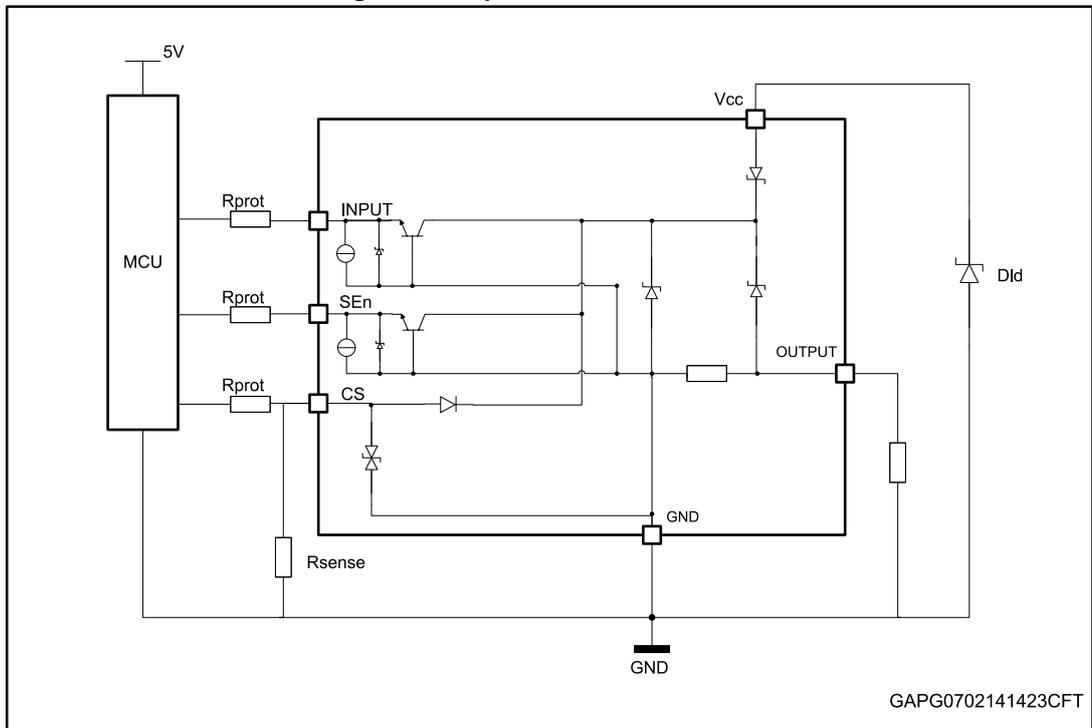
4 Application information

Figure 6: Application diagram



4.1 Protection against reverse battery

Figure 7: Simplified internal structure



The device does not need any external components to protect the internal logic in case of a reverse battery condition. The protection is provided by internal structures.

In addition, due to the fact that the output MOSFET turns on even in reverse battery mode, thus providing the same low ohmic path as in regular operating conditions, no additional power dissipation has to be considered.

4.2 Immunity against transient electrical disturbances

The immunity of the device against transient electrical emissions, conducted along the supply lines and injected into the V_{CC} pin, is tested in accordance with ISO7637-2:2011 (E) and ISO 16750-2:2010.

The related function performance status classification is shown in [Table 12: "ISO 7637-2 - electrical transient conduction along supply line"](#).

Test pulses are applied directly to DUT (Device Under Test) both in ON and OFF-state and in accordance to ISO 7637-2:2011(E), chapter 4. The DUT is intended as the present device only, without components and accessed through V_{CC} and GND terminals.

Status II is defined in ISO 7637-1 Function Performance Status Classification (FPSC) as follows: "The function does not perform as designed during the test but returns automatically to normal operation after the test".

Table 12: ISO 7637-2 - electrical transient conduction along supply line

Test Pulse 2011(E)	Test pulse severity level with Status II functional performance status		Minimum number of pulses or test time	Burst cycle / pulse repetition time		Pulse duration and pulse generator internal impedance
	Level	$U_s^{(1)}$		min	max	
1	III	-112V	500 pulses	0,5 s		2ms, 10 Ω
2a	III	+55V	500 pulses	0,2 s	5 s	50 μ s, 2 Ω
3a	IV	-220V	1h	90 ms	100 ms	0.1 μ s, 50 Ω
3b	IV	+150V	1h	90 ms	100 ms	0.1 μ s, 50 Ω
4 ⁽²⁾	IV	-7V	1 pulse			100ms, 0.01 Ω
Load dump according to ISO 16750-2:2010						
Test B ⁽³⁾		40V	5 pulse	1 min		400ms, 2 Ω

Notes:

⁽¹⁾ U_s is the peak amplitude as defined for each test pulse in ISO 7637-2:2011(E), chapter 5.6.

⁽²⁾Test pulse from ISO 7637-2:2004(E).

⁽³⁾With 40 V external suppressor referred to ground ($-40^{\circ}\text{C} < T_j < 150^{\circ}\text{C}$).

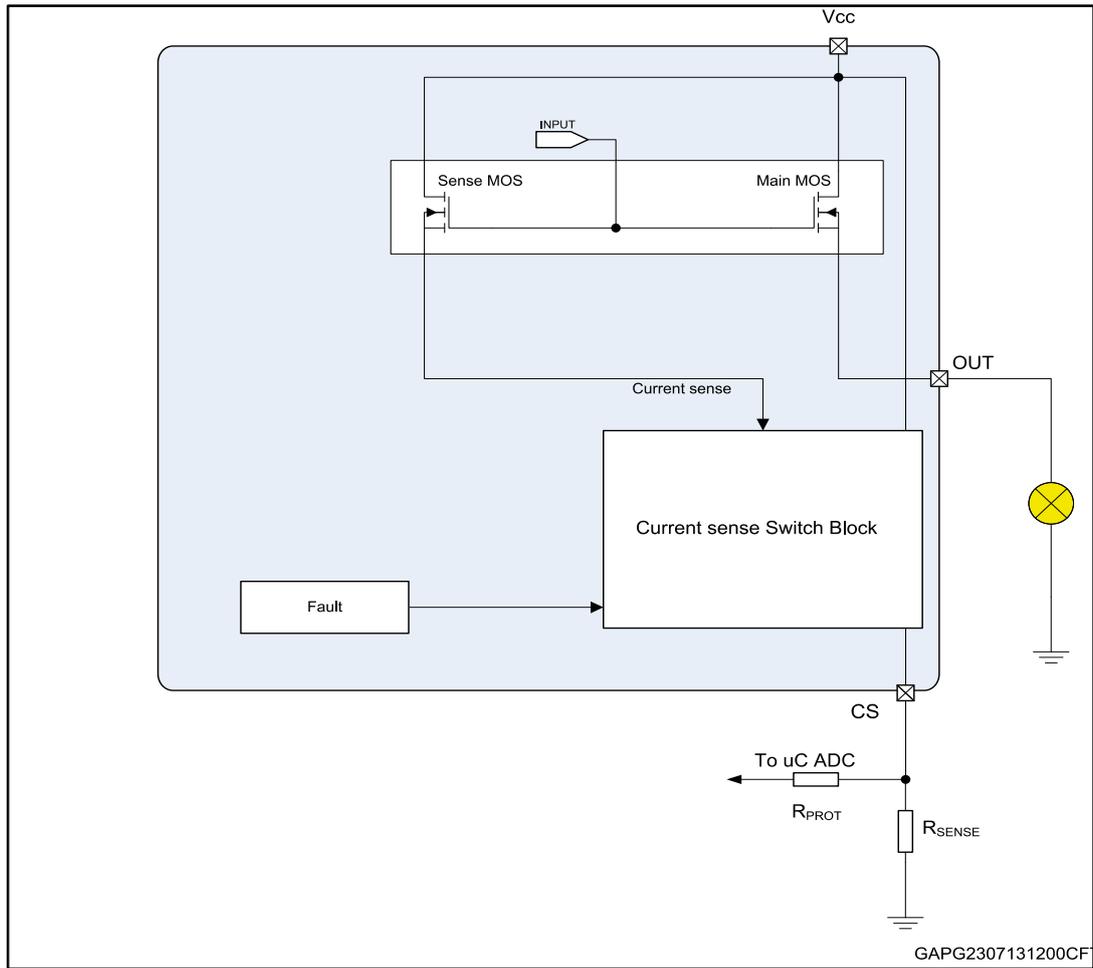
4.3 MCU I/Os protection

If a ground protection network is used and negative transients are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line both to prevent the microcontroller I/O pins from latch-up and to protect the HSD inputs.

The value of these resistors is a compromise between the leakage current of microcontroller and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of microcontroller I/Os.

4.4.1 Principle of CurrentSense signal generation

Figure 9: CurrentSense block diagram



Current sense

This output is capable of providing:

- Current mirror proportional to the load current in normal operation, delivering current proportional to the load according to known ratio named K
- Diagnostics flag in fault conditions delivering fixed voltage V_{SENSEH}

The current delivered by the current sense circuit, I_{SENSE}, can be easily converted to a voltage V_{SENSE} by using an external sense resistor, R_{SENSE}, allowing continuous load monitoring and abnormal condition detection.

Normal operation (channel ON, no fault, SEn active)

While device is operating in normal conditions (no fault intervention), V_{SENSE} calculation can be done using simple equations

Current provided by CurrentSense output: I_{SENSE} = I_{OUT}/K

Voltage on R_{SENSE}: V_{SENSE} = R_{SENSE} * I_{SENSE} = R_{SENSE} * I_{OUT}/K

Where :

- V_{SENSE} is voltage measurable on R_{SENSE} resistor

- I_{SENSE} is current provided from CS pin in current output mode
- I_{OUT} is current flowing through output
- K factor represents the ratio between PowerMOS cells and SenseMOS cells; its spread includes geometric factor spread, current sense amplifier offset and process parameters spread of overall circuitry specifying ratio between I_{OUT} and I_{SENSE} .

Failure flag indication

In case of power limitation/overtemperature, the fault is indicated by the CS pin which is switched to a “current limited” voltage source, V_{SENSEH} .

In any case, the current sourced by the CS in this condition is limited to I_{SENSEH}

Figure 10: Analogue HSD – open-load detection in off-state

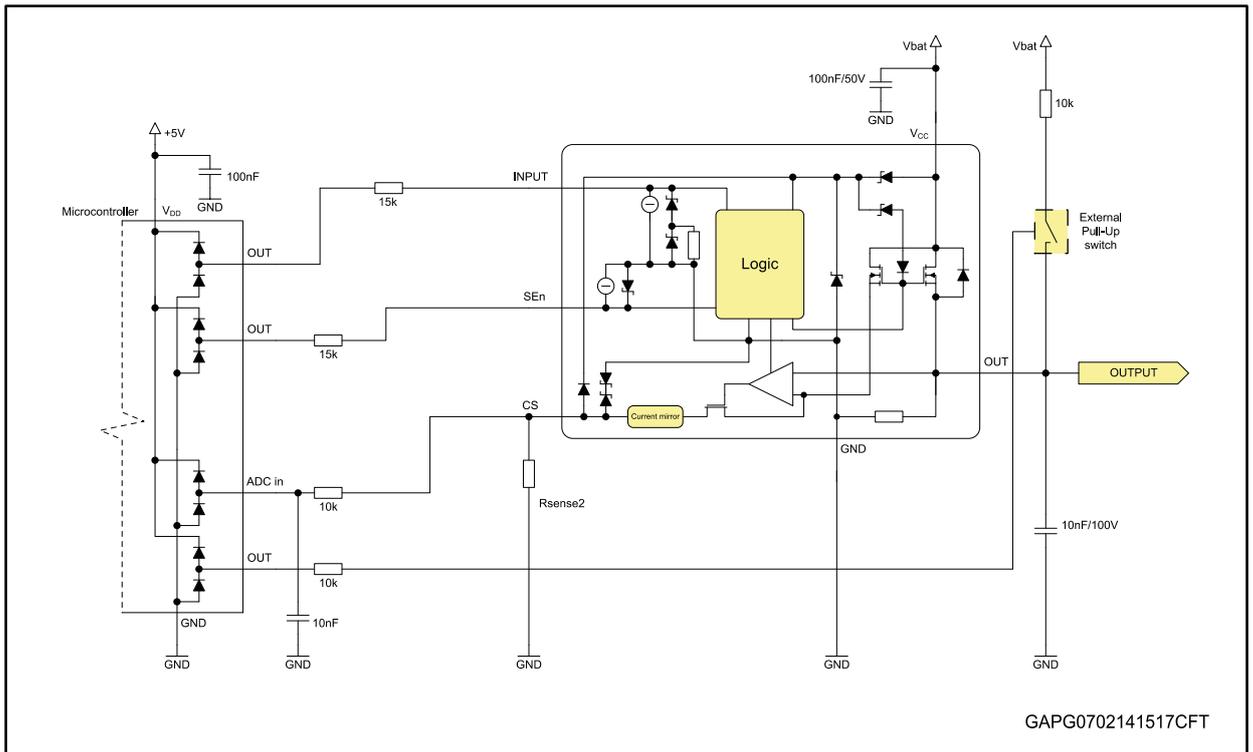


Figure 11: Open-load / short to VCC condition

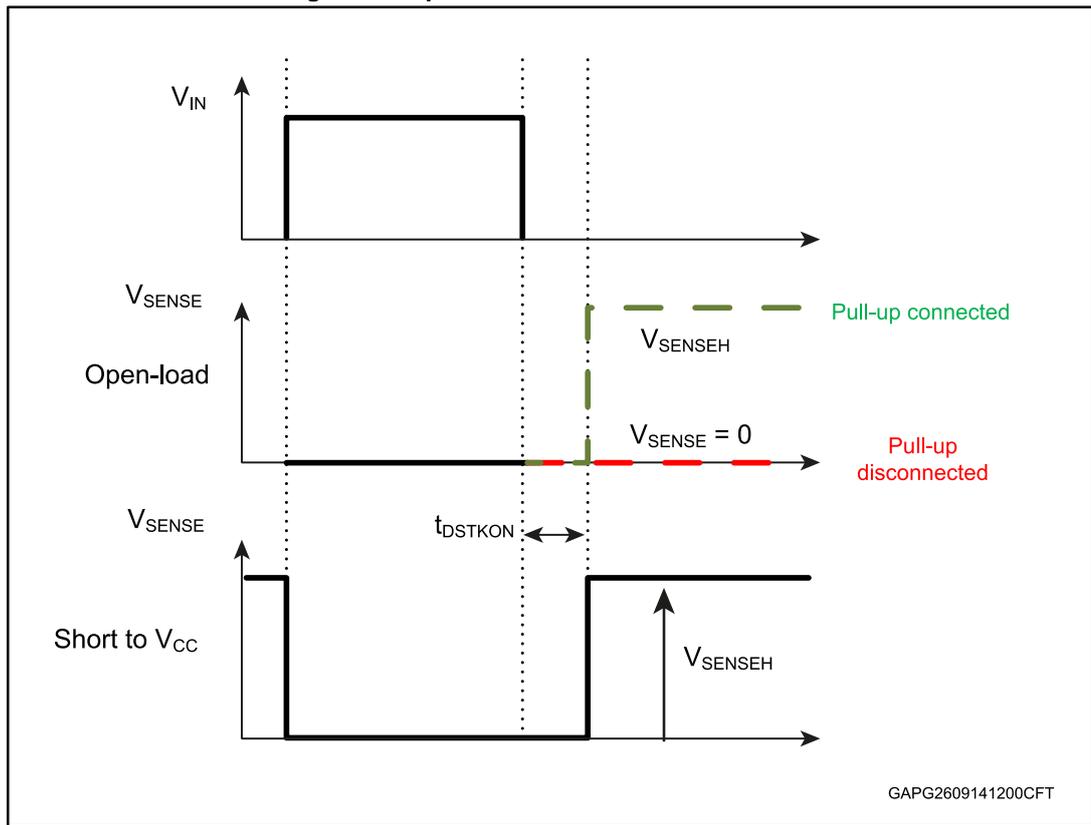


Table 13: CurrentSense pin levels in off-state

Condition	Output	CurrentSense	SEn
Open-load	$V_{OUT} > V_{OL}$	Hi-Z	L
		V_{SENSEH}	H
	$V_{OUT} < V_{OL}$	Hi-Z	L
		0	H
Short to V_{CC}	$V_{OUT} > V_{OL}$	Hi-Z	L
		V_{SENSEH}	H
Nominal	$V_{OUT} < V_{OL}$	Hi-Z	L
		0	H

4.4.2 Short to VCC and OFF-state open-load detection

Short to V_{CC}

A short circuit between V_{CC} and output is indicated by the relevant current sense pin set to V_{SENSEH} during the device off-state. Small or no current is delivered by the current sense during the on-state depending on the nature of the short circuit.

OFF-state open-load with external circuitry

Detection of an open-load in off mode requires an external pull-up resistor R_{PU} connecting the output to a positive supply voltage V_{PU} .

It is preferable V_{PU} to be switched off during the module standby mode in order to avoid the overall standby current consumption to increase in normal conditions, i.e. when load is connected.

R_{PU} must be selected in order to ensure $V_{OUT} > V_{OLmax}$ in accordance with the following equation:

Equation

$$R_{PU} < \frac{V_{PU} - 4}{I_{L(off2)min @ 4V}}$$

5 Package and PCB thermal data

5.1 Octapak thermal data

Figure 12: Octapak on two-layers PCB (2s0p to JEDEC JESD 51-5)

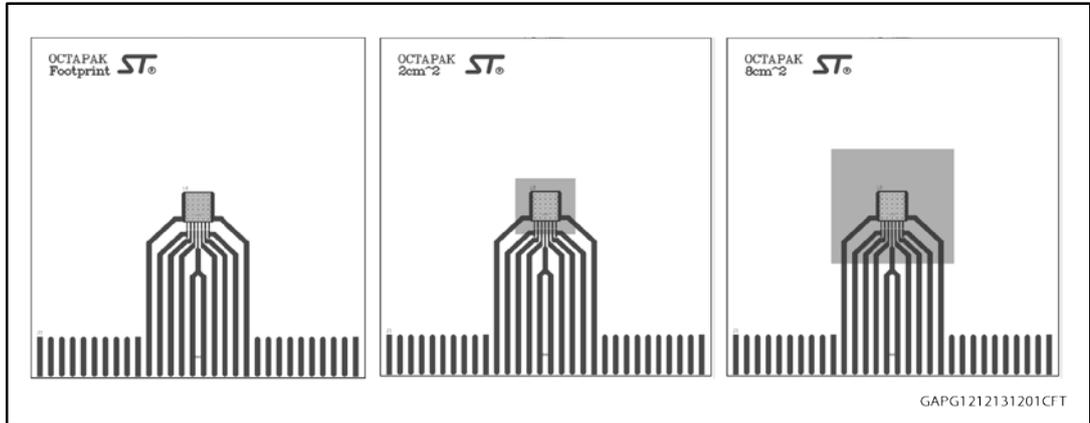


Figure 13: Octapak on four-layers PCB (2s2p to JEDEC JESD 51-7)

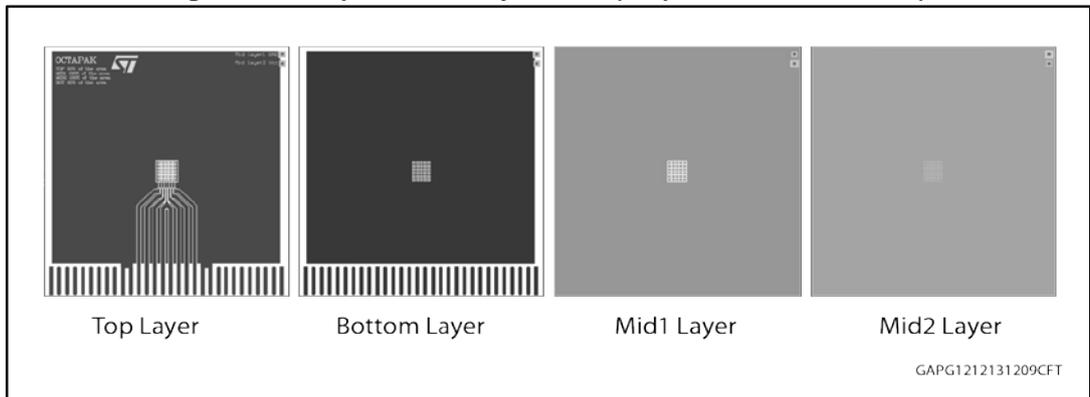


Table 14: PCB properties

Dimension	Value
Board finish thickness	1.6 mm +/- 10%
Board dimension	77 mm x 86 mm
Board Material	FR4
Copper thickness (top and bottom layers)	0.070 mm
Copper thickness (inner layers)	0.035 mm
Thermal vias separation	1.2 mm
Thermal via diameter	0.3 mm +/- 0.08 mm
Copper thickness on vias	0.025 mm
Footprint dimension (top layer)	6.4 mm x 7mm
Heatsink copper area dimension (bottom layer)	Footprint, 2 cm ² or 8 cm ²

Figure 14: Rthj-amb vs PCB copper area in open box free air conditions

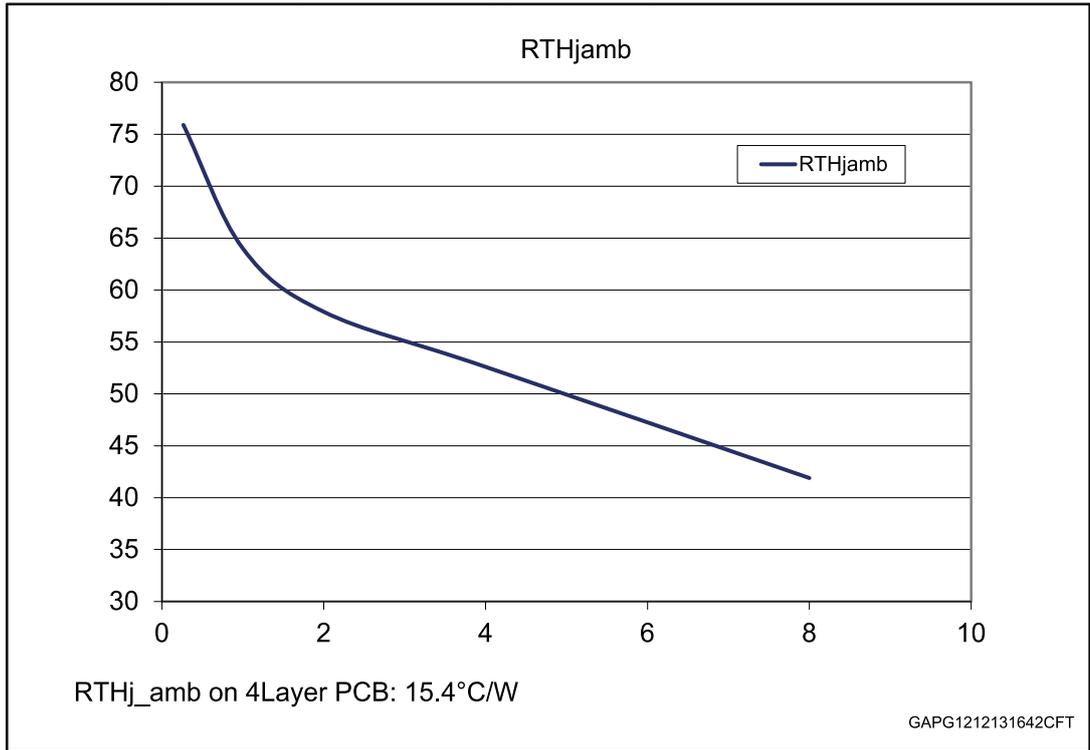
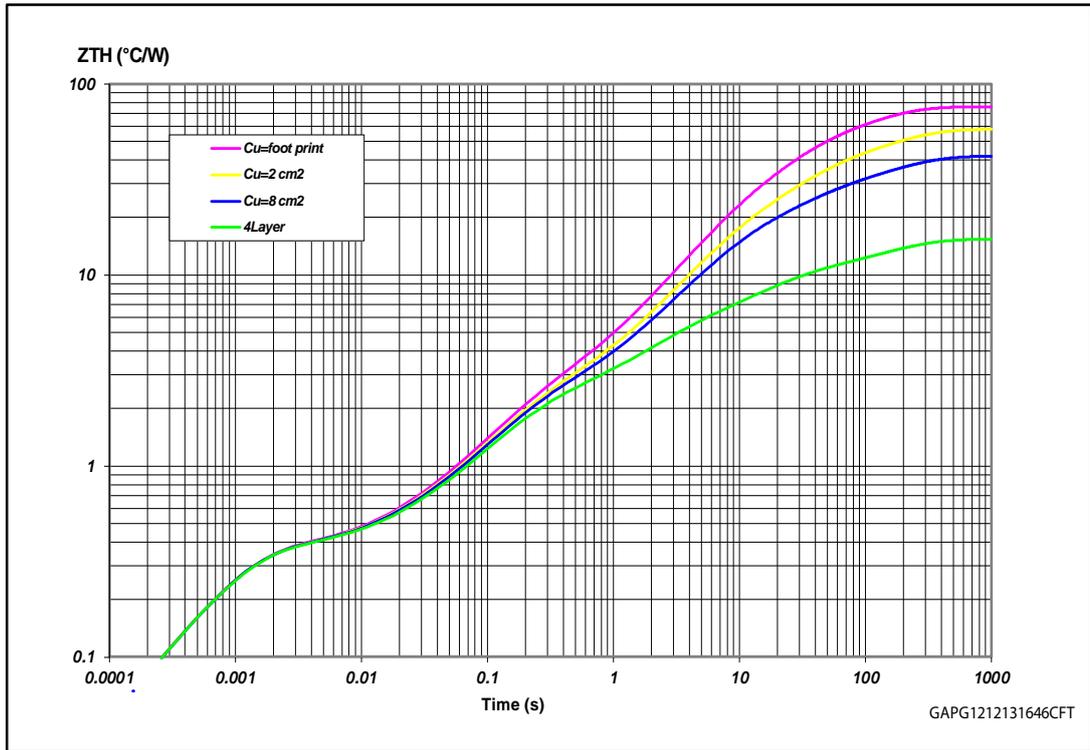


Figure 15: Octapak thermal impedance junction ambient single pulse

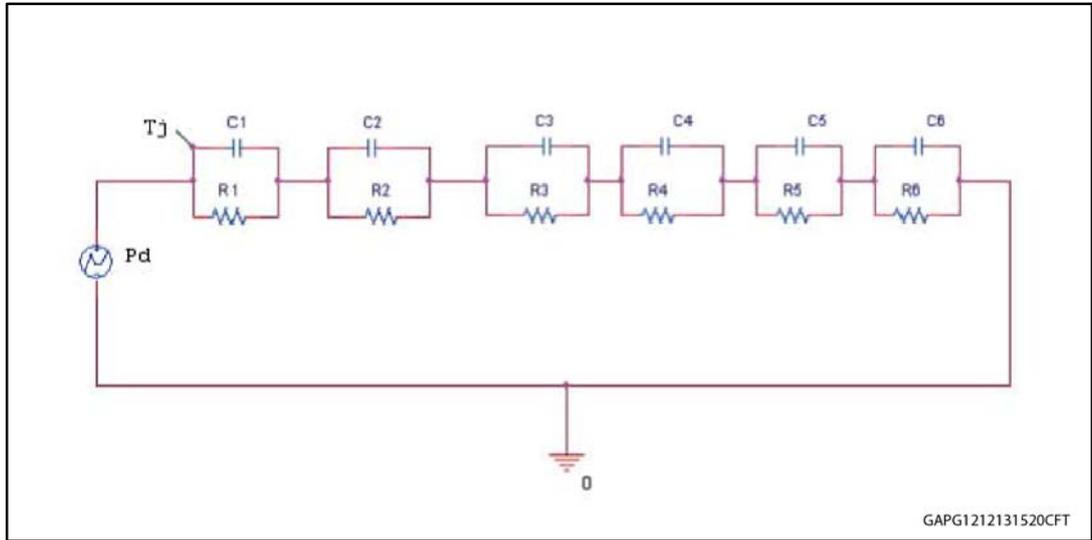


Equation: Pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot + Z_{THtp} (1 - \delta)$$

where $\delta = t_p/T$

Figure 16: Thermal fitting model for Octapak



The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Table 15: Thermal parameters

Area/island (cm ²)	Footprint	2	8	4L
R1 (°C/W)	0.005	0.005	0.005	0.005
R2 (°C/W)	0.35	0.35	0.35	0.35
R3 (°C/W)	1.54	1.54	1.54	1.54
R4 (°C/W)	10	10	10	2.5
R5 (°C/W)	28	20	12	5
R6 (°C/W)	36	26	18	6
C1 (W.s/°C)	0.002	0.002	0.002	0.002
C2 (W.s/°C)	0.0025	0.0025	0.0025	0.0025
C3 (W.s/°C)	0.1	0.1	0.1	0.1
C4 (W.s/°C)	0.6	0.6	0.6	0.8
C5 (W.s/°C)	0.8	1.4	2.2	3
C6 (W.s/°C)	3	6	9	25

6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

6.1 Octapak package information

Figure 17: Octapak package dimensions

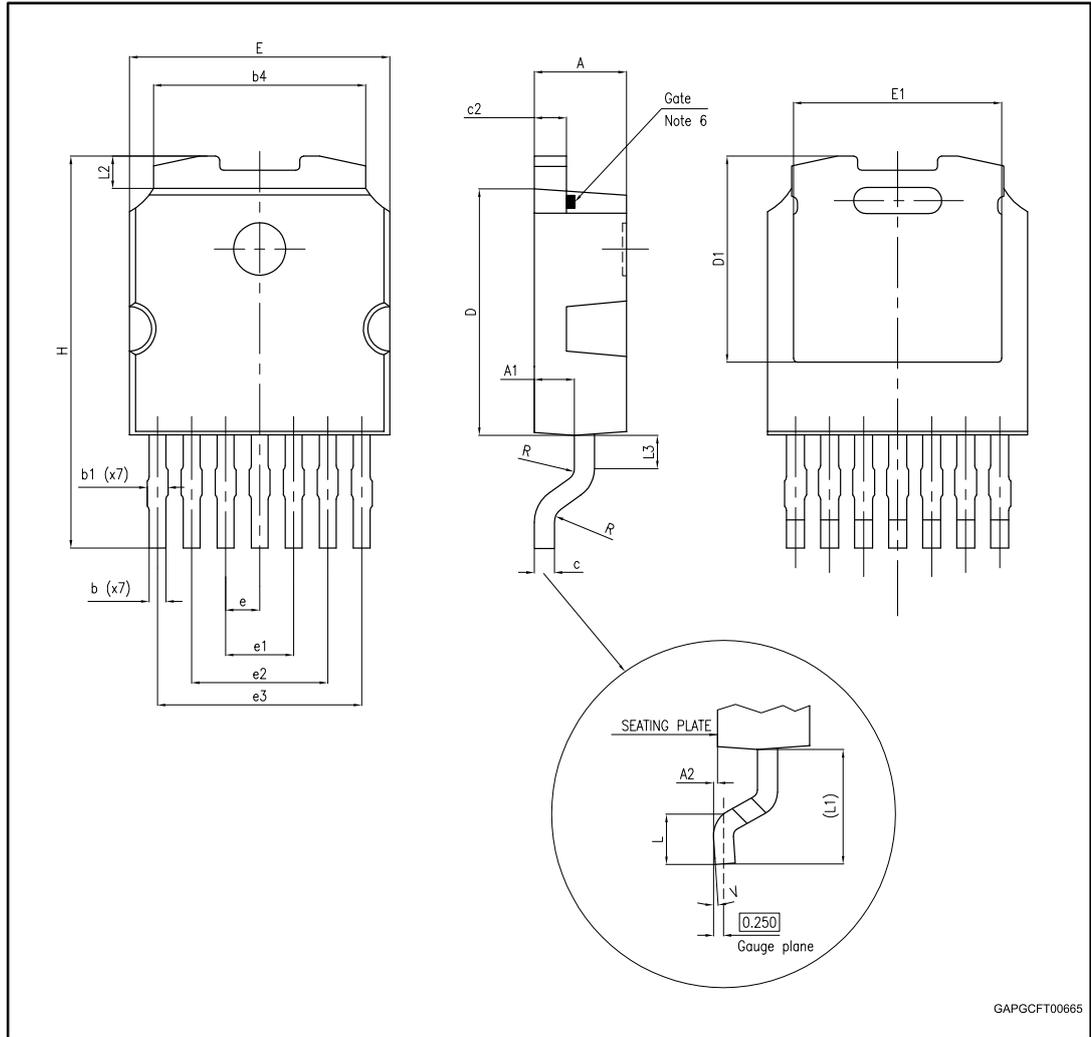


Table 16: Octapak mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A	2.20	2.30	2.40
A1	0.90	1.00	1.10
A2	0.03		0.15
b	0.38	0.45	0.52
b1			0.70
b4	5.20	5.30	5.40
c	0.45	0.50	0.60
c2	0.75	0.80	0.90
D	6.00	6.10	6.20
D1		5.15	
E	6.40	6.50	6.60
E1		5.30	
e	0.85 BSC		
e1	1.60	1.70	1.80
e2	3.30	3.40	3.50
e3	5.00	5.10	5.20
H	9.35	9.70	10.10
L	1.00		—
(L1)		2.80	
L2		0.80	
L3		0.85	
R	0.40 BSC		
V2	0°		8°

6.2 Octapak packing information

Figure 18: Octapak reel 13"

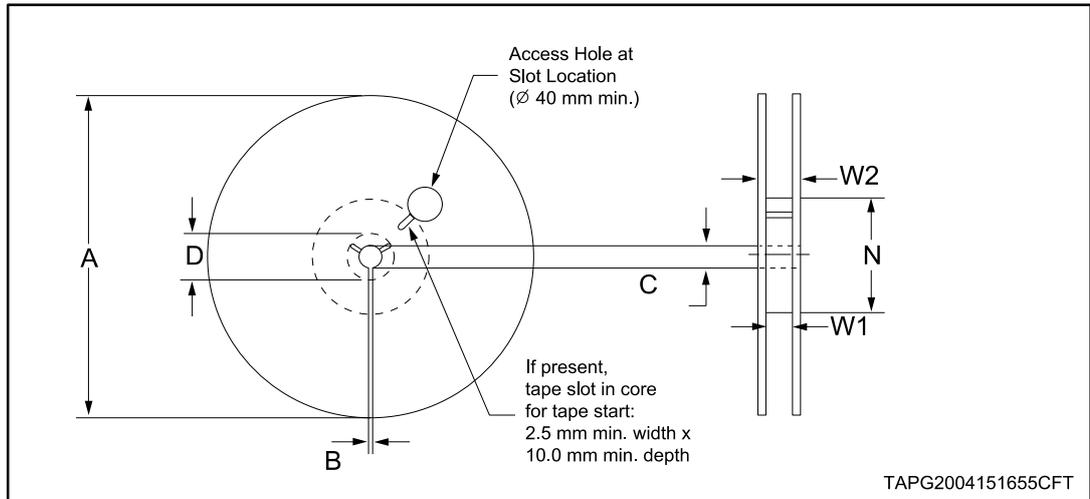


Table 17: Reel dimensions

Description	Value ⁽¹⁾
Base quantity	2500
Bulk quantity	2500
A (max)	330
B (min)	1.5
C (+0.5, -0.2)	13
D	20.2
N	100
W1 (+2 /-0)	16.4
W2 (max)	22.4

Notes:

⁽¹⁾All dimensions are in mm.

Figure 19: Octapak carrier tape

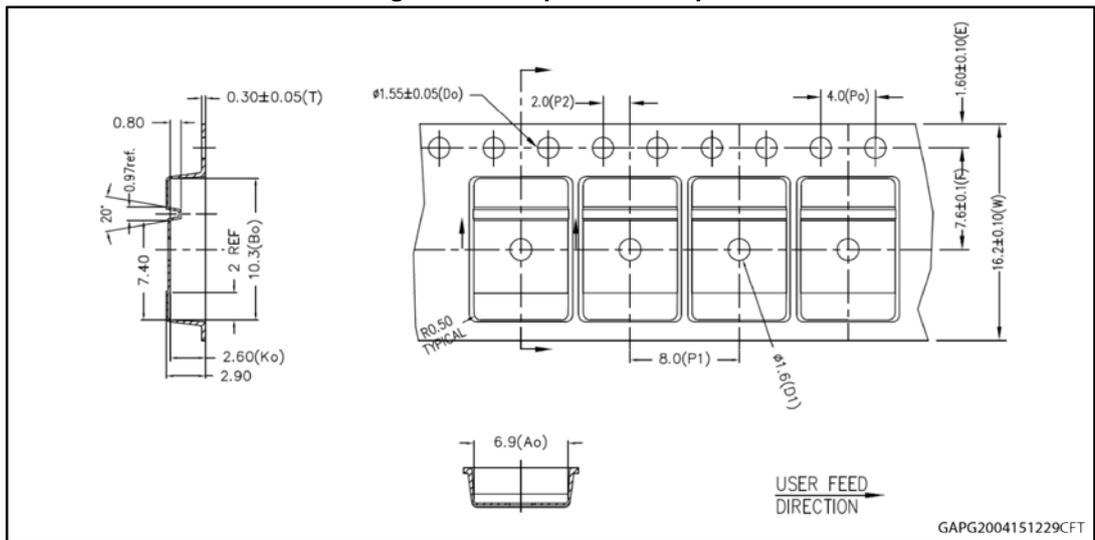
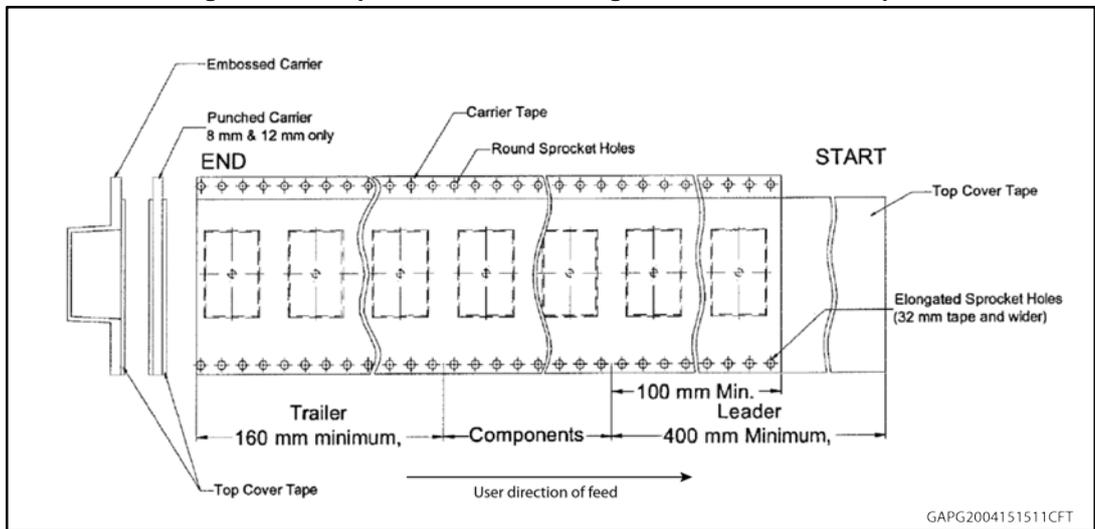
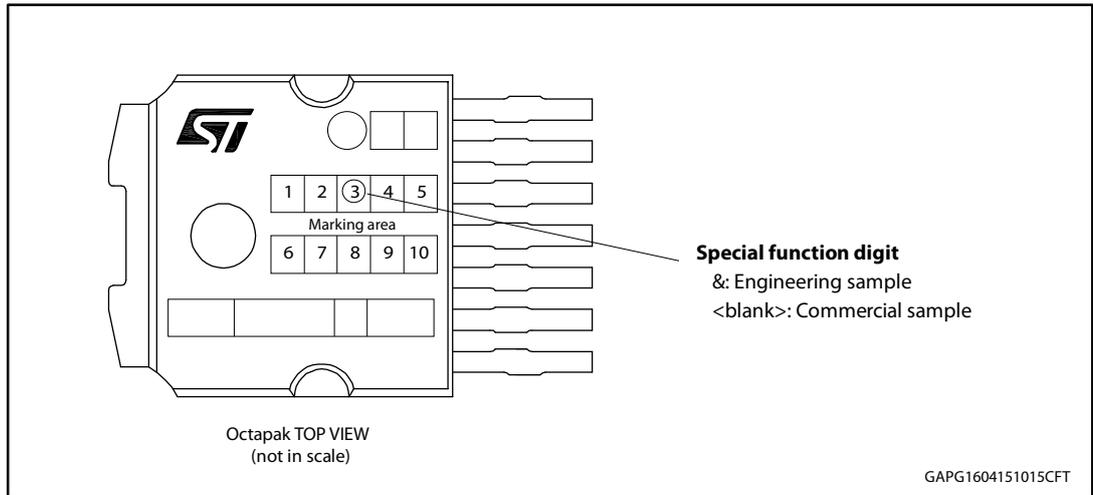


Figure 20: Octapak schematic drawing of leader and trailer tape



6.3 Octapak marking information

Figure 21: Octapak marking information



Parts marked as "&" are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

7 Revision history

Table 18: Document revision history

Date	Revision	Changes
21-Apr-2015	1	Initial release
06-Aug-2015	2	<p><i>Table 4: "Absolute maximum ratings":</i></p> <ul style="list-style-type: none"> • V_{CC_LSC}: removed row • E_{MAX}: updated value <p><i>Table 6: "Power section":</i></p> <ul style="list-style-type: none"> • I_{STBY}, $I_{L(off)}$: updated values <p>Updated <i>Table 7: "Switching"</i></p> <p><i>Table 9: "Protection":</i></p> <ul style="list-style-type: none"> • I_{LIMH}: updated values <p><i>Table 10: "CurrentSense":</i></p> <ul style="list-style-type: none"> • K_x, dK_x/K_x, I_{SENSE0}, I_{OUT_SAT}: updated values
12-Nov-2015	3	<p>Updated <i>Section "Features"</i></p> <p><i>Table 6: "Power section":</i></p> <ul style="list-style-type: none"> • I_{STBY}, $I_{L(off)}$: updated values <p><i>Table 10: "CurrentSense":</i></p> <ul style="list-style-type: none"> • dK_x/K_x: updated values
27-Apr-2016	4	<p>Updated <i>Figure 1: "Block diagram"</i></p> <p><i>Table 10: "CurrentSense":</i></p> <ul style="list-style-type: none"> • K_3: updated values

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2016 STMicroelectronics – All rights reserved