SAM G55 Series Family
Silicon Errata and Data Sheet Clarification

The SAM G55 Series family of devices that you have received conform functionally to the current Device Data Sheet (Atmel-11289F-ATARM-SAM-G55G-SAM-G55J-Datasheet_27-May-16), except for the anomalies described in this document.

New Silicon Errata Issues

Note:	This document provides information on new errata issues for the SAM G55 Series of devices. Please refer to the current device data sheet for all pre-existing silicon errata issues.

There are no new silicon errata to report at this time.

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the Device Data Sheet (Atmel-11289F-ATARM-SAM-G55G-SAM-G55J-Datasheet_27-May-16).

Corrections in tables and paragraphs are shown in **bold.** Where possible, the original bold text formatting has been removed for the clarity.

1. Module: Bootloader

Chapter 7 “Bootloader” has new verbiage for the NRST line. The newly added text is shown in bold.

The SAM G55 devices ship with a factory-programmed bootoader in Flash. The Flash loader downloads code either through the SPI or through the TWI0.

The Bootloader mode is entered automatically on power-up if no valid firmware is detected in the Flash. A valid firmware is detected by performing a CRC on the content of the Flash. If the CRC is correct, the application is started. Otherwise, the Bootloader mode is entered.

Alternatively, the Bootloader mode can be forced by applying 10 low pulses of 1 ms on the NRST line (with a period of 10 ms max). When the bootloader detects this sequence, it asserts the pin PA01 (NCHG) low as an acknowledge.

The Bootloader mode initializes the TWI0 in Slave Mode with the I^2C address 0x26 and the SPI in Slave Mode, 8-bit data length, SPI Mode 1.

2. Module: CCFG_USBMR Register

In the current data sheet section 15.9.7, the PLLFREQADJUST bit is missing from the register description. This bit occupies a bit offset of 4 as shown below.

PLLFREQADJUST: USB PLL output automatic synchronization

0:USB PLL clock is not adjust

1:USB PLL output is automatically adjust at 48 MHz +/-0.25% whatever the internal 32 KHz accuracy.

3. Module: CKGR_PLLAR Register

In the current data sheet section 18.20.9, the MULA bit field for the CKGR_PLLAR register extends from bit 16 to bit 27. The corrected bit field extends from bit 16 to bit 28.

4. Module: CKGR_PLLBR Register

In the current data sheet, the MULB bit field for the CKGR_PLLBR register extends from bit field 16 to 26. The corrected bit field extended from 16 to 27.

5. Module: PMC_PMMR Register

In the current data sheet Section 18.20.32, the PLLA_MMAX bit field for the PMC_PMMR register extends from bit 0 to bit 10. The corrected bit field extends from bit 0 to bit 12.

6. Module: PMC_PMMR Register

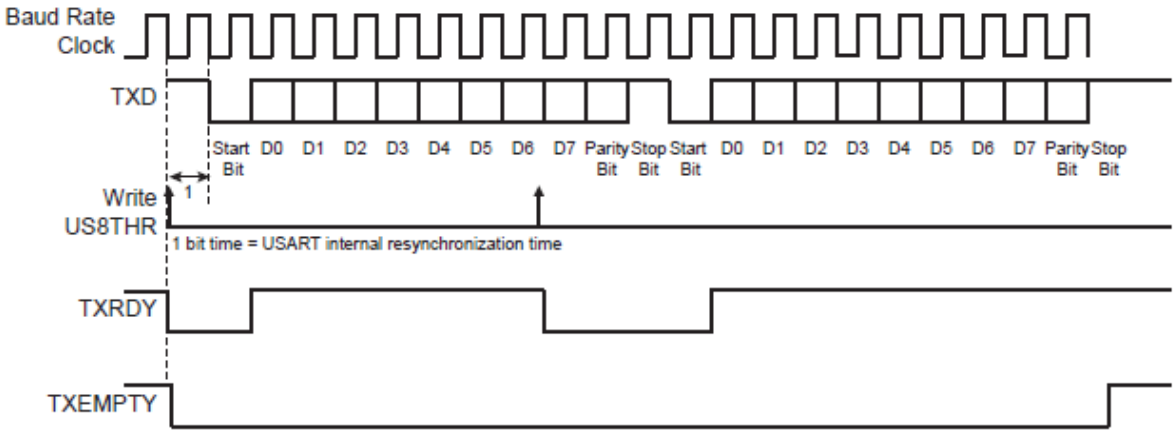
In the current data sheet Section 18.20.32, the PLLB_MMAX bit field for the PMC_PMMR register extends from bit 16 to bit 26. The corrected bit field extends from bit 16 to bit 27.

7. Module: I2SC_MR Register

The table for the FORMAT bit in the Section 33.8.2 is incorrect and lists Left-Justified format. This format is not supported for this device.

8. Module: Transmitter Operations

Figure 30-6 is incorrect. The corrected figure is as follows:



9. Module: Multidrop Mode

In the Section 30.6.3.6, the bit name SENTA is incorrect. The corrected name is SENDA.

10. Module: ISO7816 Mode Overview

The last paragraph of the Section 30.6.4.1 has erroneous text. The corrected text is given in bold.

When operating in ISO7816, either in T = 0 or T = 1 modes, the character format is fixed. The configuration is 8 data bits and 1 or 2 stop bits, regardless of the values programmed in the Mode register fields CHRL, MODE9 and CHMODE. MSBF can be used to transmit LSB or MSB first. The Parity (PAR) bit can be used to transmit in normal or inverse mode. Refer to Section 31.7.3 “USART Mode Register” and “PAR: Parity Type”.

11. Module: US_RTOR Register

In the Section 30.7.20, the TimeOut (TO) bit information is incomplete, hence the following information has been added.

TimeOut (TO) value is 17 bits for USART, which supports all modes including LIN Mode.

16 bits for USART which supports all modes.

8 bits for USART which does not support ISO7816.

12. Module: US_LINMR Register

The following sentence in the Section 30.7.25 has an error and should be disregarded:

This register can only be written if the WPEN bit is cleared in the USART Write Protection Mode Register.

APPENDIX A: REVISION HISTORY

Revision A Document (07/2019)

This is the initial released version of this document.

Note the following details of the code protection feature on Microchip devices:

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