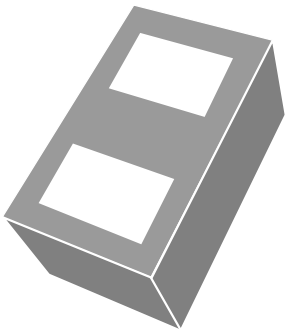
# ESDALC20-1BF4

## Low clamping, low capacitance bidirectional single line ESD protection

**Datasheet - production data**



**0201 package**

## Features

- Low $V_{BR}/V_{CL}$ ratio
- Bidirectional device
- Low leakage current < 1 nA typ.
- 0201 package
- Ultra low PCB area: 0.18 $mm^2$
- ECOPACK®2 compliant component

### Complies with the following standards

- IEC 61000-4-2 level 4:
  - ±30 kV (air discharge)
  - ±20 kV (contact discharge)

## Applications

Where transient over voltage protection in ESD sensitive equipment is required, such as:

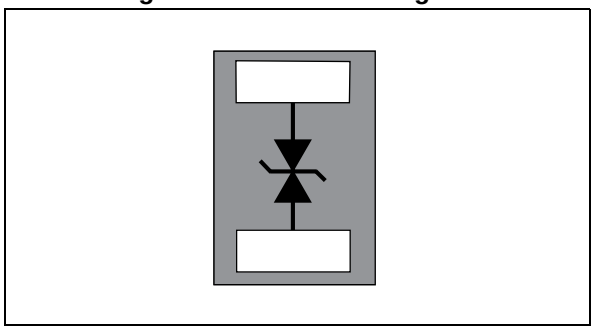
- Smartphones, mobile phones and accessories
- Tablet, PC, netbooks and notebooks
- Portable multimedia devices and accessories
- Digital cameras and camcorders
- Communication and highly integrated systems

## Description

The ESDALC20-1BF4 is a bidirectional single line TVS diode designed to protect the data line or other I/O ports against ESD transients.

The device is ideal for applications where both reduced line capacitance and board space saving are required.

**Figure 1. Functional diagram**





This is information on a product in full production. www.st.com

# 1 Characteristics

**Table 1. Absolute maximum ratings**

| Symbol | Parameter | | Value | Unit |
|---|---|---|---|---|
| $V_{PP}$ (1) | Peak pulse voltage | IEC 61000-4-2 contact discharge<br>IEC 61000-4-2 air discharge | 20<br>30 | kV |
| $P_{PP}$ (1) | Peak pulse power (8/20 µs) | | 90 | W |
| $I_{PP}$ (1) | Peak pulse current (8/20 µs) | | 2.4 | A |
| $T_j$ | Operating junction temperature range | | -40 to 150 | °C |
| $T_{stg}$ | Storage temperature range | | -65 to +150 | °C |
| $T_L$ | Maximum lead temperature for soldering during 10 s | | 260 | °C |

1. For a surge greater than the maximum values, the diode will fail in short-circuit.

**Figure 2. Electrical characteristics (definitions)**

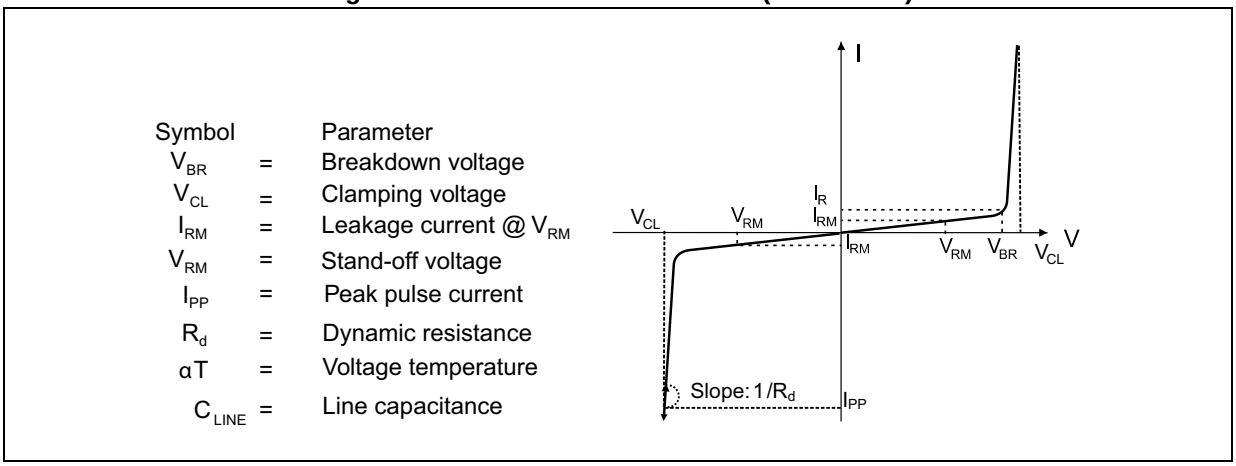



**Table 2. Electrical characteristics (values, $T_{amb}$ = 25 °C)**

| Symbol | Test conditions | Value | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| $V_{BR}$ | $I_R$ = 1 mA | 22 | 23 | | V |
| $I_{RM}$ | $V_{RM}$ = 20 V | | < 1 | 10 | nA |
| $V_{RM}$ | Stand-off voltage | -20 | | 20 | V |
| $V_{CL}$ | 8 kV contact discharge after 30 ns ($I_{PP}$ = 16 A), IEC 61000-4-2 | | 37 | | V |
| $C_{LINE}$ | $V_{LINE}$= 0 V, F = 1 MHz, $V_{OSC}$ = 30 mV | | 10.5 | 11.5 | pF |

**Figure 3. Leakage current versus junction temperature (typical values)**

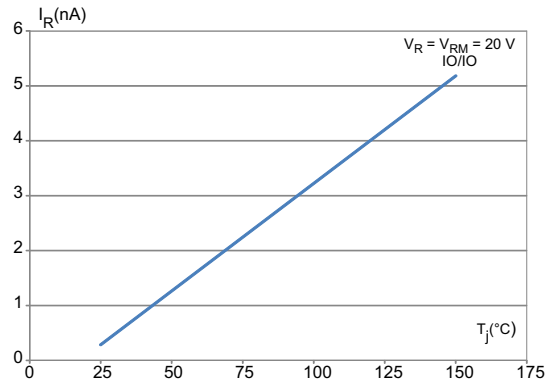



**Figure 4. Junction capacitance versus applied voltage (typical values)**

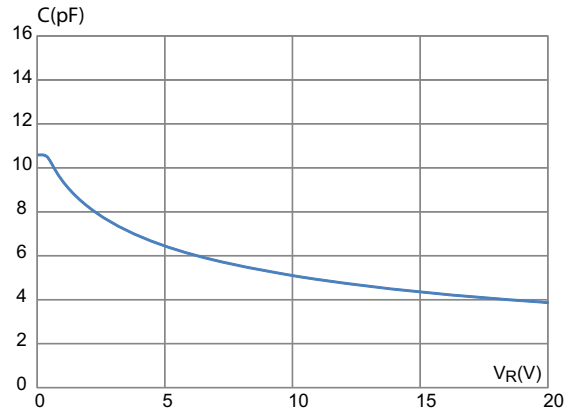



**Figure 5. ESD response to IEC 61000-4-2 (+8 kV contact discharge)**

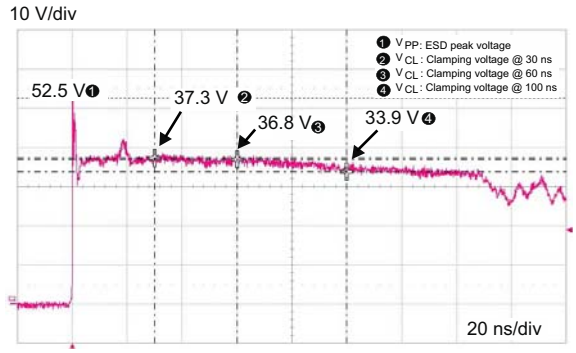



**Figure 6. ESD response to IEC 61000-4-2 (-8 kV contact discharge)**

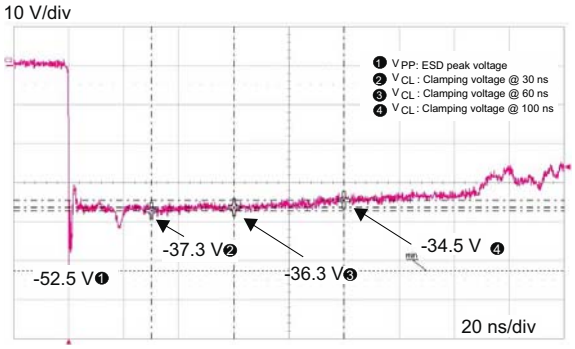



**Figure 7. Dynamic resistance**

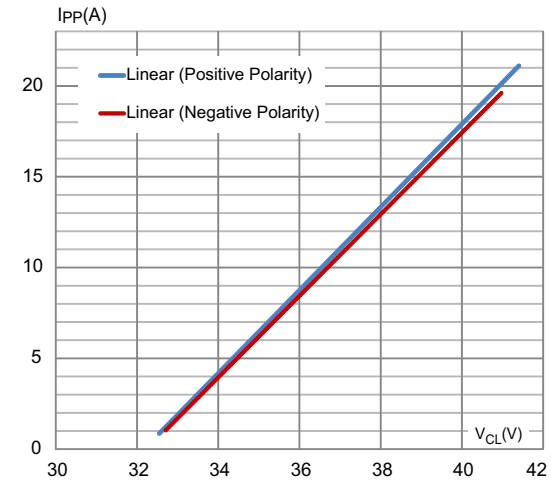
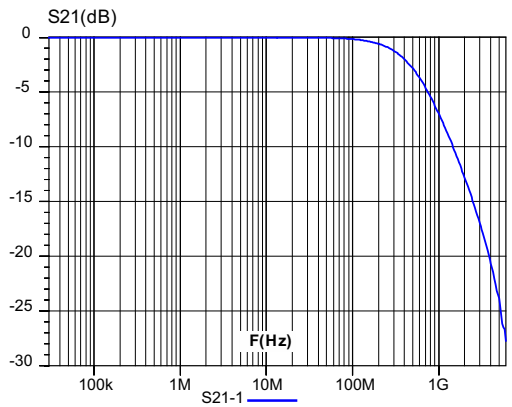



**Figure 8. S21 attenuation measurement result**



# 2 Package information

- Epoxy meets UL94, V0
- Lead-free package

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com.* ECOPACK® is an ST trademark.

## 2.1 0201 package information

**Figure 9. 0201 package outline**

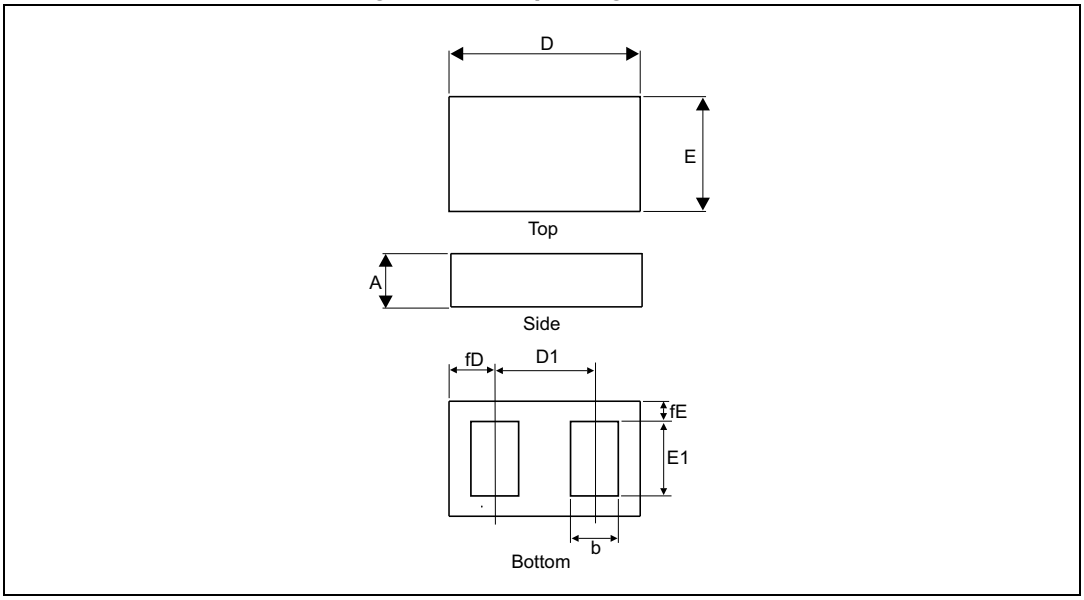



**Table 3. 0201 package mechanical data**

| Ref. | Dimensions | | | | | |
|---|---|---|---|---|---|---|
| | Millimeters | | | Inches | | |
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | 0.28 | 0.3 | 0.32 | 0.0110 | 0.0118 | 0.0126 |
| b | 0.125 | 0.14 | 0.155 | 0.0049 | 0.0055 | 0.0061 |
| D | 0.57 | 0.6 | 0.63 | 0.0224 | 0.0236 | 0.0248 |
| D1 | | 0.35 | | | 0.0138 | |
| E | 0.27 | 0.3 | 0.33 | 0.0106 | 0.0118 | 0.0130 |
| E1 | 0.175 | 0.19 | 0.205 | 0.0069 | 0.0075 | 0.0081 |
| fD | 0.11 | 0.125 | 0.014 | 0.0043 | 0.0049 | 0.0055 |
| fE | 0.04 | 0.055 | 0.07 | 0.0016 | 0.0022 | 0.0028 |

Figure 10. Footprint in mm (inches)

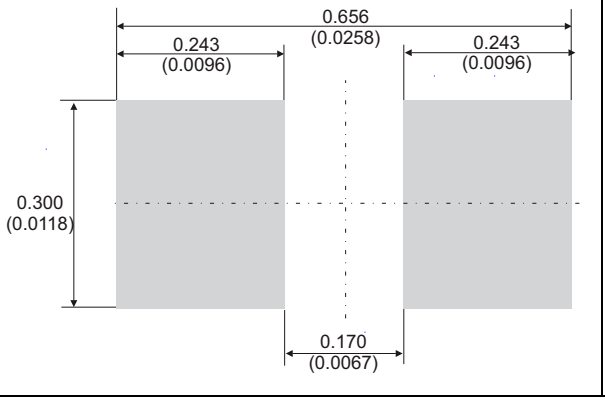
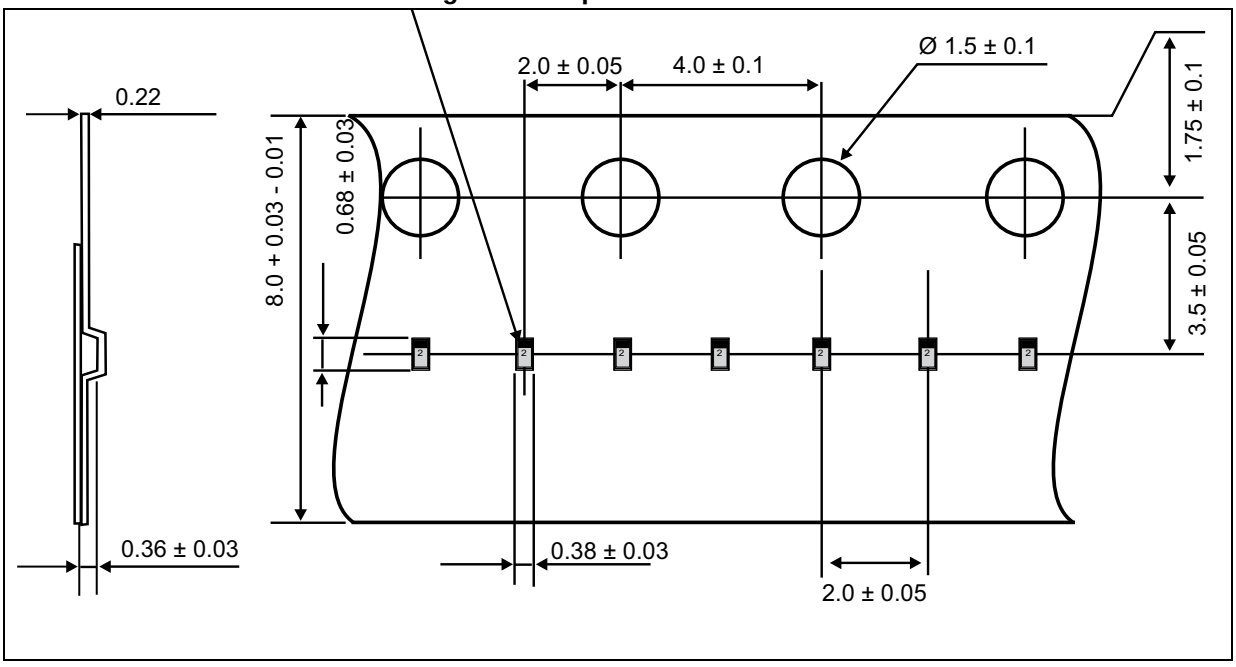



Figure 11. Marking

*Note: The marking codes can be rotated by 90° or 180° to differentiate assembly location.In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.*

## 2.2 Packing information

Figure 12. Tape and reel outline

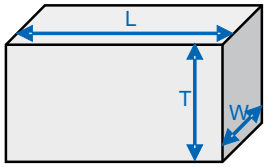


# 3 Recommendation on PCB assembly

## 3.1 Stencil opening design

1. General recommendations on stencil opening design
   a) Stencil opening dimensions: L (Length), W (Width), T (Thickness).

**Figure 13. Stencil opening dimensions**



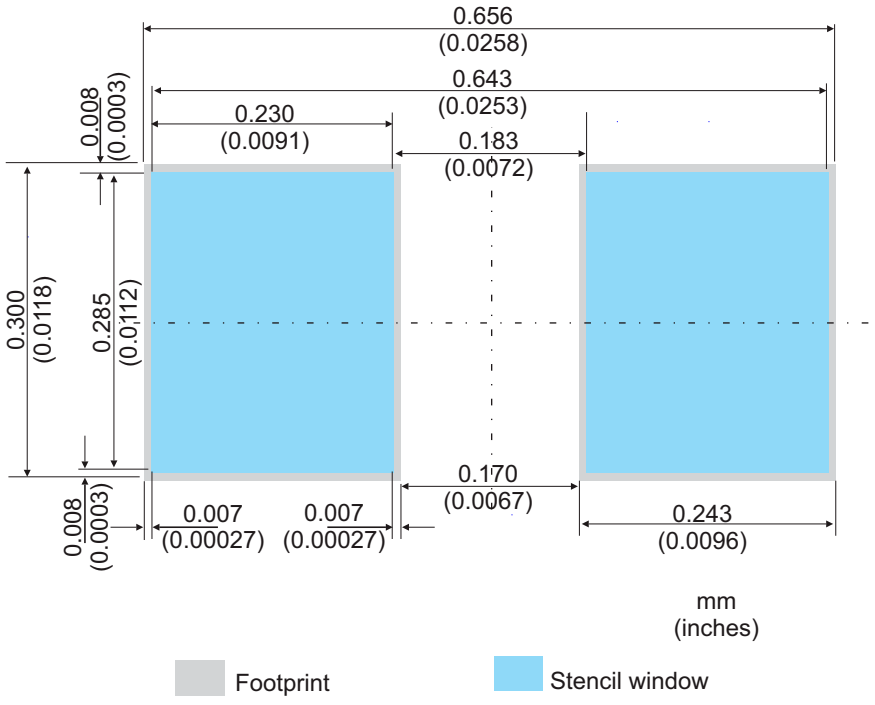

   b) General design rule
   Stencil thickness (T) = 75 ~ 125 µm

$$\text{Aspect Ratio} = \frac{W}{T} \geq 1.5$$

$$\text{Aspect Area} = \frac{L \times W}{2T(L + W)} \geq 0.66$$

2. Recommended stencil window
   a) Stencil opening thickness: 80 µm
   b) Other dimensions: see *Figure 14*

**Figure 14. Recommended stencil window position, stencil opening thickness: 80 µm**



## 3.2 Solder paste

1. Use halide-free flux, qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste recommended.
3. Offers a high tack force to resist component displacement during PCB movement.
4. Use solder paste with fine particles: Type 4 (powder particle size 20-48 µm per IPC J STD-005).

## 3.3 Placement

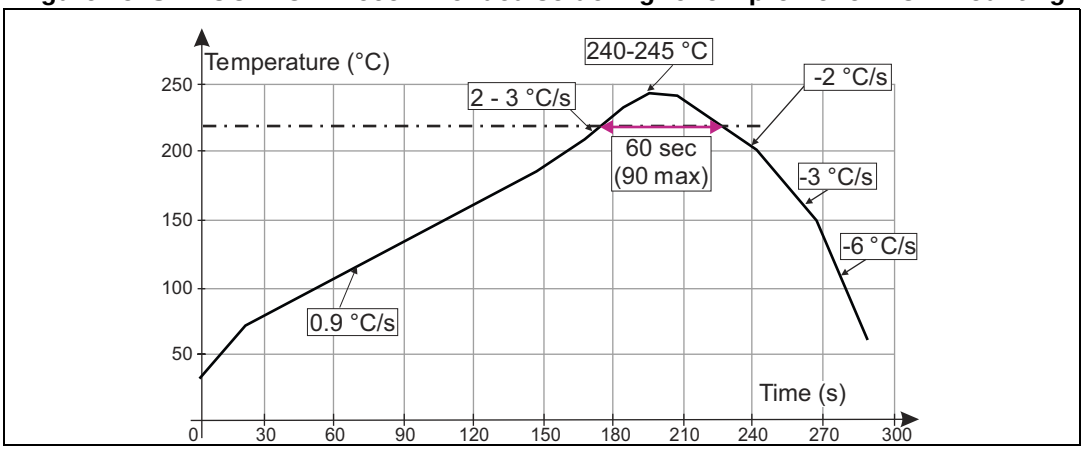
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering.
3. Standard tolerance of ± 0.05 mm is recommended.
4. 1.0 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

## 3.4 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. The symmetrical layout is recommended, in case any tilt phenomena caused by asymmetrical solder paste amount due to the solder flow away.

## 3.5 Reflow profile

**Figure 15. ST ECOPACK® recommended soldering reflow profile for PCB mounting**




*Note: Minimize air convection currents in the reflow oven to avoid component movement.*

# 4 Ordering information

**Figure 16. Ordering information scheme**

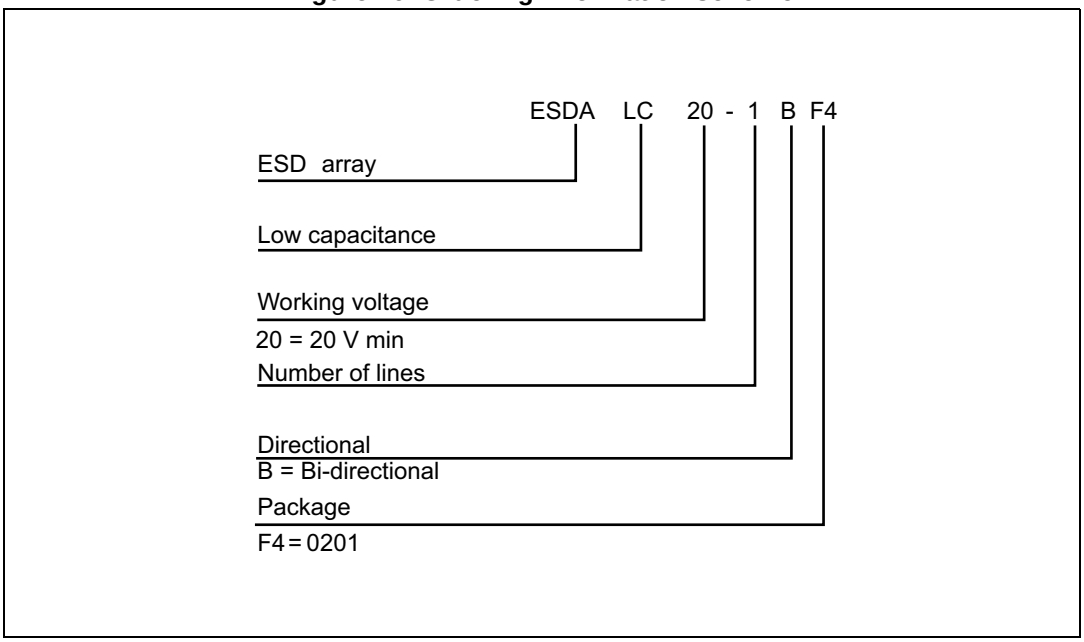



**Table 4. Ordering information**

| Order code | Marking | Package | Weight | Base qty | Delivery mode |
|---|---|---|---|---|---|
| ESDALC20-1BF4 | 2(1) | 0201 | 0.116 mg | 15000 | Tape and reel |

1. The marking codes can be rotated by 90° or 180° to differentiate assembly location

# 5 Revision history

**Table 5. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 23-Jul-2015 | 1 | First issue |

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