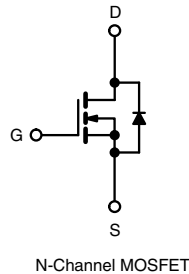
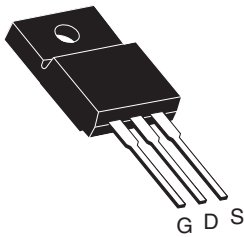


## Power MOSFET

| PRODUCT SUMMARY           |                 |      |
|---------------------------|-----------------|------|
| $V_{DS}$ (V)              | 100             |      |
| $R_{DS(on)}$ ( $\Omega$ ) | $V_{GS} = 10$ V | 0.54 |
| $Q_g$ (Max.) (nC)         | 8.3             |      |
| $Q_{gs}$ (nC)             | 2.3             |      |
| $Q_{gd}$ (nC)             | 3.8             |      |
| Configuration             | Single          |      |

**TO-220 FULLPAK**

**FEATURES**

- Isolated Package
- High Voltage Isolation = 2.5 kV<sub>RMS</sub> (t = 60 s; f = 60 Hz)
- Sink to Lead Creepage Distance = 4.8 mm
- 175 °C Operating Temperature
- Dynamic dV/dt Rating
- Low Thermal Resistance
- Compliant to RoHS Directive 2002/95/EC


 Available  
**RoHS\***  
 COMPLIANT

**DESCRIPTION**

Third Generation Power MOSFETs from Vishay provides the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost effectiveness.

The TO-220 FULLPAK eliminates the need for additional insulating hardware in commercial-industrial applications. The moulding compound used provides a high isolation capability and a low thermal resistance between the tab and external heatsink. This isolation is equivalent to using a 100 micron mica barrier with standard TO-220 product. The FULLPAK is mounted to a heatsink using a single clip or by a single screw fixing.

**ORDERING INFORMATION**

|                |                |
|----------------|----------------|
| Package        | TO-220 FULLPAK |
| Lead (Pb)-free | IRFI510GPbF    |
|                | SiHFI510G-E3   |
| SnPb           | IRFI510G       |
|                | SiHFI510G      |

**ABSOLUTE MAXIMUM RATINGS** ( $T_C = 25$  °C, unless otherwise noted)

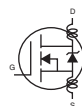
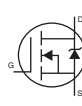
| PARAMETER  | SYMBOL           | LIMIT            | UNIT  |          |
|--|------------------|------------------|-------|----------|
| Drain-Source Voltage                             | $V_{DS}$         | 100              | V     |          |
| Gate-Source Voltage                              | $V_{GS}$         | $\pm 20$         |       |          |
| Continuous Drain Current                         | $V_{GS}$ at 10 V | $T_C = 25$ °C    | A     |          |
|  |                  | $T_C = 100$ °C   |       |          |
| Pulsed Drain Current <sup>a</sup>                | $I_{DM}$         | 18               |       |          |
| Linear Derating Factor                           |                  | 0.18             | W/°C  |          |
| Single Pulse Avalanche Energy <sup>b</sup>       | $E_{AS}$         | 60               | mJ    |          |
| Repetitive Avalanche Current <sup>a</sup>        | $I_{AR}$         | 4.5              | A     |          |
| Repetitive Avalanche Energy <sup>a</sup>         | $E_{AR}$         | 2.7              | mJ    |          |
| Maximum Power Dissipation                        | $T_C = 25$ °C    | $P_D$            | 27    | W        |
| Peak Diode Recovery dV/dt <sup>c</sup>           | dV/dt            | 4.5              | V/ns  |          |
| Operating Junction and Storage Temperature Range | $T_J, T_{stg}$   | - 55 to + 175    | °C    |          |
| Soldering Recommendations (Peak Temperature)     | for 10 s         | 300 <sup>d</sup> |       |          |
| Mounting Torque                                  | 6-32 or M3 screw | 10               |       | lbf · in |
|  |                  | 1.1              | N · m |          |

**Notes**

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 25$  V, starting  $T_J = 25$  °C, L = 4.4 mH,  $R_g = 25$   $\Omega$ ,  $I_{AS} = 4.5$  A (see fig. 12).
- $I_{SD} \leq 5.6$  A,  $dI/dt \leq 75$  A/ $\mu$ s,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 175$  °C.
- 1.6 mm from case.

\* Pb containing terminations are not RoHS compliant, exemptions may apply

| THERMAL RESISTANCE RATINGS       |            |      |      |      |
|----------------------------------|------------|------|------|------|
| PARAMETER                        | SYMBOL     | TYP. | MAX. | UNIT |
| Maximum Junction-to-Ambient      | $R_{thJA}$ | -    | 65   | °C/W |
| Maximum Junction-to-Case (Drain) | $R_{thJC}$ | -    | 5.5  |      |

| SPECIFICATIONS ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted) |                     |   |      |      |           |               |
|---|---------------------|---|------|------|-----------|---------------|
| PARAMETER   | SYMBOL              | TEST CONDITIONS   | MIN. | TYP. | MAX.      | UNIT          |
| <b>Static</b>   |                     |   |      |      |           |               |
| Drain-Source Breakdown Voltage  | $V_{DS}$            | $V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$   | 100  | -    | -         | V             |
| $V_{DS}$ Temperature Coefficient  | $\Delta V_{DS}/T_J$ | Reference to $25\text{ }^\circ\text{C}$ , $I_D = 1\text{ mA}$   | -    | 0.63 | -         | V/°C          |
| Gate-Source Threshold Voltage   | $V_{GS(th)}$        | $V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$   | 2.0  | -    | 4.0       | V             |
| Gate-Source Leakage   | $I_{GSS}$           | $V_{GS} = \pm 20$   | -    | -    | $\pm 100$ | nA            |
| Zero Gate Voltage Drain Current   | $I_{DSS}$           | $V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}$  | -    | -    | 25        | $\mu\text{A}$ |
|   |                     | $V_{DS} = 80\text{ V}, V_{GS} = 0\text{ V}, T_J = 150\text{ }^\circ\text{C}$  | -    | -    | 250       |               |
| Drain-Source On-State Resistance  | $R_{DS(on)}$        | $V_{GS} = 10\text{ V}, I_D = 2.7\text{ A}^b$  | -    | -    | 0.54      | $\Omega$      |
| Forward Transconductance  | $g_{fs}$            | $V_{DS} = 50\text{ V}, I_D = 2.7\text{ A}^b$  | 1.2  | -    | -         | S             |
| <b>Dynamic</b>  |                     |   |      |      |           |               |
| Input Capacitance   | $C_{iss}$           | $V_{GS} = 0\text{ V}$<br>$V_{DS} = 25\text{ V}$<br>$f = 1.0\text{ MHz}$ , see fig. 5  | -    | 180  | -         | pF            |
| Output Capacitance  | $C_{oss}$           |   | -    | 81   | -         |               |
| Reverse Transfer Capacitance  | $C_{rss}$           |   | -    | 15   | -         |               |
| Drain to Sink Capacitance   | $C$                 |   | -    | 12   | -         |               |
| Total Gate Charge   | $Q_g$               | $V_{GS} = 10\text{ V}, I_D = 5.6\text{ A}, V_{DS} = 80\text{ V}$ ,<br>see fig. 6 and 13 <sup>b</sup>  | -    | -    | 8.3       | nC            |
| Gate-Source Charge  | $Q_{gs}$            |   | -    | -    | 2.3       |               |
| Gate-Drain Charge   | $Q_{gd}$            |   | -    | -    | 3.8       |               |
| Turn-On Delay Time  | $t_{d(on)}$         | $V_{DD} = 50\text{ V}, I_D = 5.6\text{ A}$<br>$R_g = 24\text{ }\Omega, R_D = 8.4\text{ }\Omega$ , see fig. 10 <sup>b</sup>                                      | -    | 6.9  | -         | ns            |
| Rise Time   | $t_r$               |   | -    | 16   | -         |               |
| Turn-Off Delay Time   | $t_{d(off)}$        |   | -    | 15   | -         |               |
| Fall Time   | $t_f$               |   | -    | 9.4  | -         |               |
| Internal Drain Inductance   | $L_D$               | Between lead,<br>6 mm (0.25") from<br>package and center of<br>die contact  | -    | 4.5  | -         | nH            |
| Internal Source Inductance  | $L_S$               |   | -    | 7.5  | -         |               |
| <b>Drain-Source Body Diode Characteristics</b>                              |                     |   |      |      |           |               |
| Continuous Source-Drain Diode Current                                       | $I_S$               | MOSFET symbol<br>showing the<br>integral reverse<br>p - n junction diode    | -    | -    | 4.5       | A             |
| Pulsed Diode Forward Current <sup>a</sup>                                   | $I_{SM}$            |   | -    | -    | 18        |               |
| Body Diode Voltage  | $V_{SD}$            | $T_J = 25\text{ }^\circ\text{C}, I_S = 4.5\text{ A}, V_{GS} = 0\text{ V}^b$   | -    | -    | 2.5       | V             |
| Body Diode Reverse Recovery Time  | $t_{rr}$            | $T_J = 25\text{ }^\circ\text{C}, I_F = 5.6\text{ A}, di/dt = 100\text{ A}/\mu\text{s}^b$  | -    | 100  | 200       | ns            |
| Body Diode Reverse Recovery Charge  | $Q_{rr}$            |   | -    | 0.44 | 0.88      | $\mu\text{C}$ |
| Forward Turn-On Time  | $t_{on}$            | Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )   |      |      |           |               |

**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .

## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

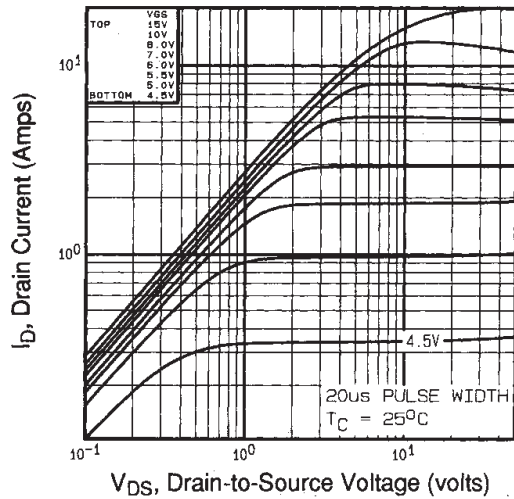


Fig. 1 - Typical Output Characteristics,  $T_C = 25\text{ }^\circ\text{C}$

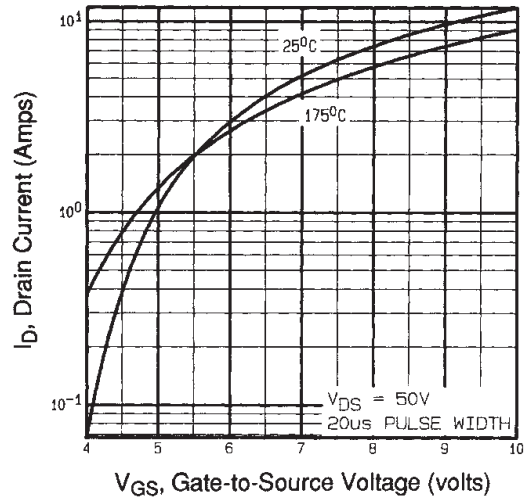


Fig. 3 - Typical Transfer Characteristics

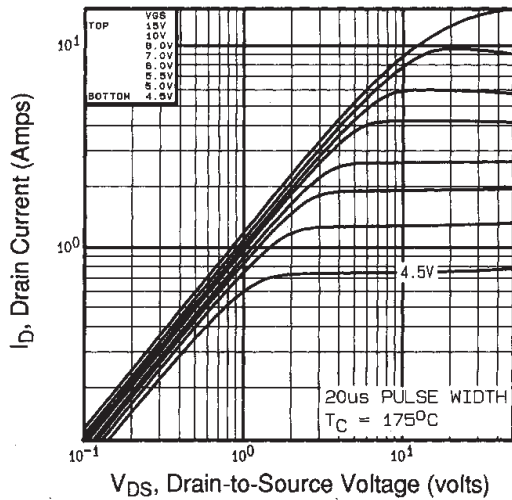


Fig. 2 - Typical Output Characteristics,  $T_C = 175\text{ }^\circ\text{C}$

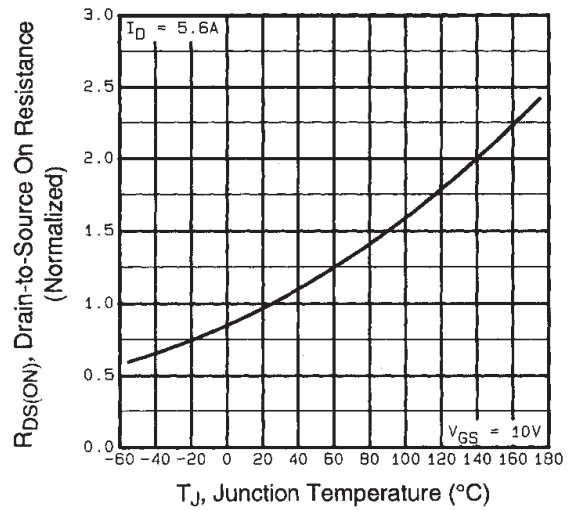


Fig. 4 - Normalized On-Resistance vs. Temperature

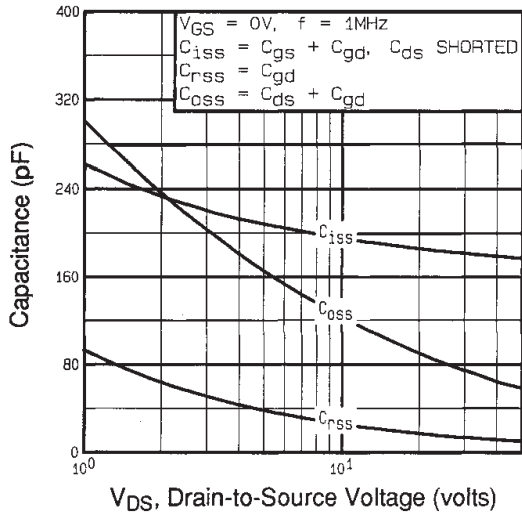


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

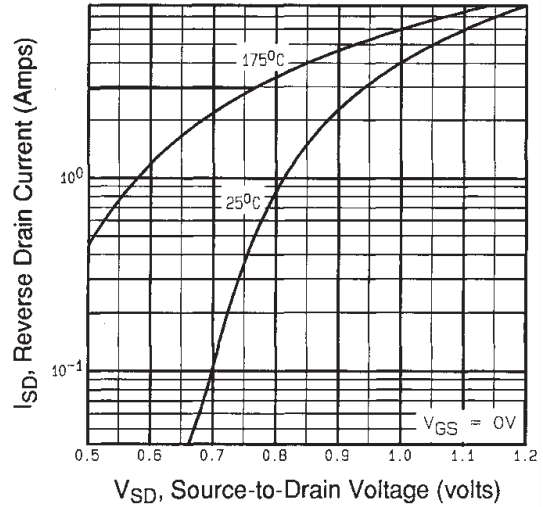


Fig. 7 - Typical Source-Drain Diode Forward Voltage

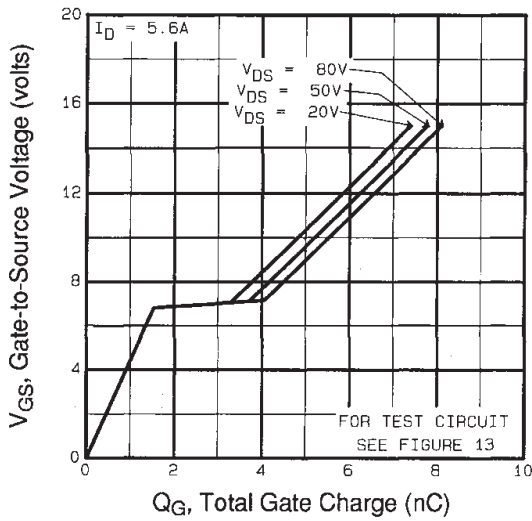


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

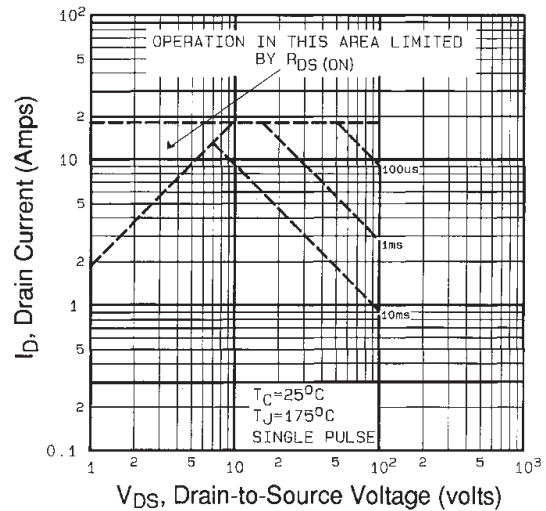


Fig. 8 - Maximum Safe Operating Area

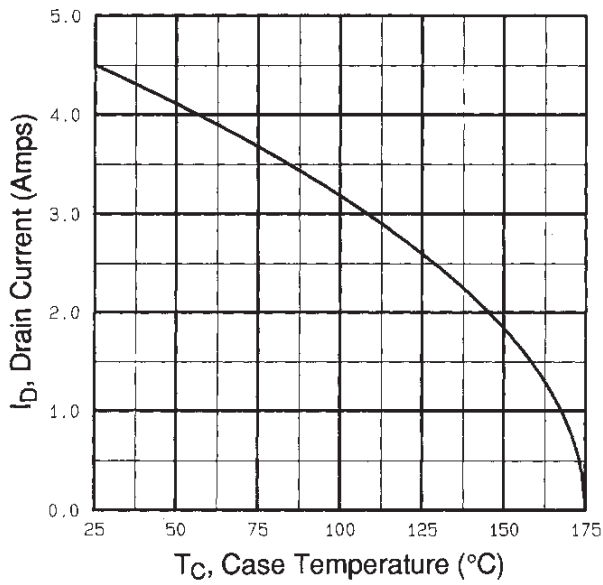


Fig. 9 - Maximum Drain Current vs. Case Temperature

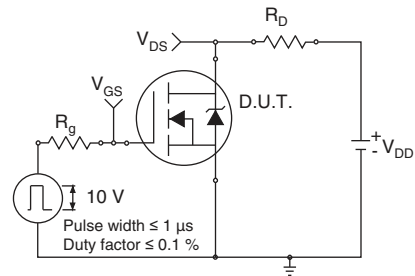


Fig. 10a - Switching Time Test Circuit

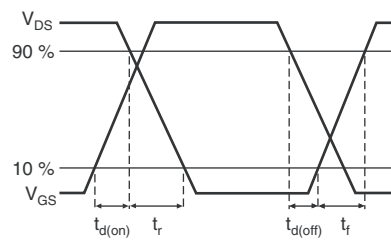


Fig. 10b - Switching Time Waveforms

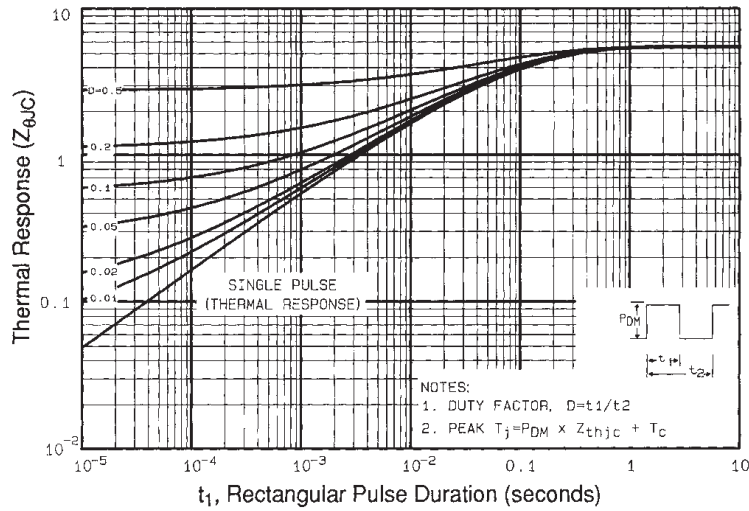


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

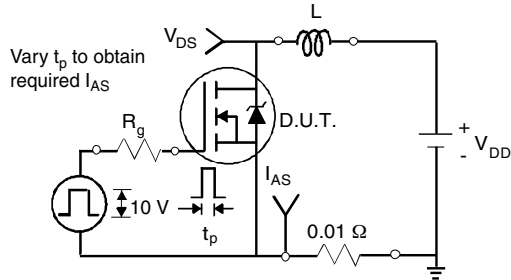


Fig. 12a - Unclamped Inductive Test Circuit

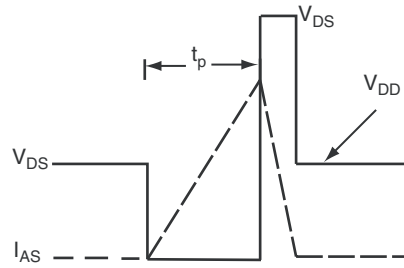


Fig. 12b - Unclamped Inductive Waveforms

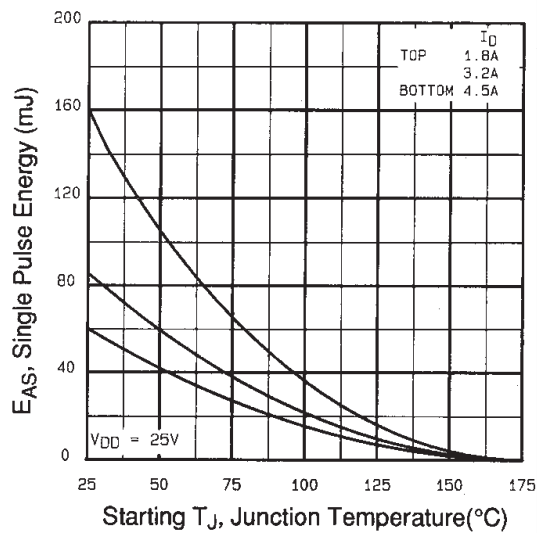


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

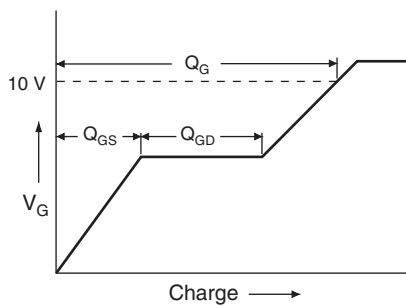


Fig. 13a - Basic Gate Charge Waveform

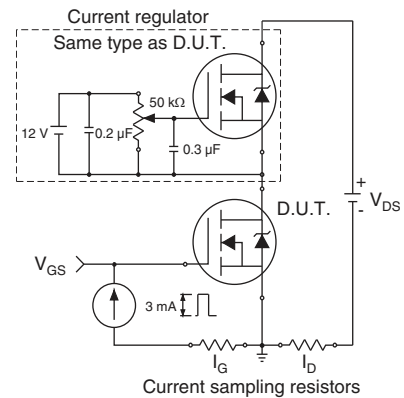
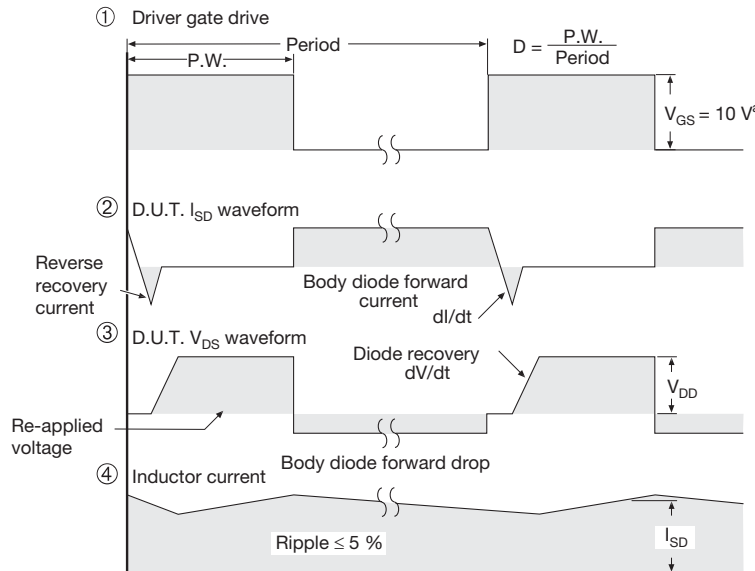
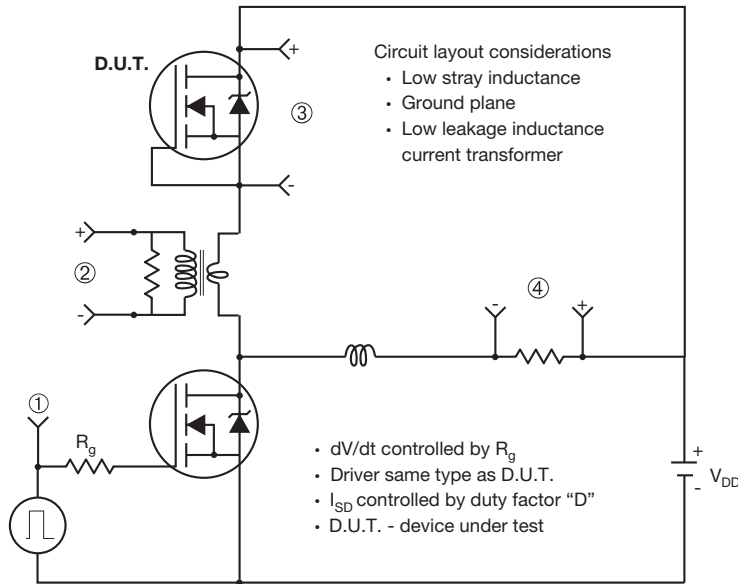


Fig. 13b - Gate Charge Test Circuit

### Peak Diode Recovery dV/dt Test Circuit



**Note**

a.  $V_{GS} = 5 V$  for logic level devices

**Fig. 14 - For N-Channel**

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