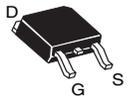


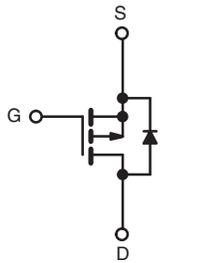
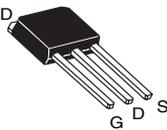
Power MOSFET

PRODUCT SUMMARY	
V_{DS} (V)	- 200
$R_{DS(on)}$ (Ω)	$V_{GS} = - 10$ V 1.5
Q_g (Max.) (nC)	20
Q_{gs} (nC)	3.3
Q_{gd} (nC)	11
Configuration	Single

DPAK (TO-252)



IPAK (TO-251)



P-Channel MOSFET

FEATURES

- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- Surface Mount (IRFR9220, SiHFR9220)
- Straight Lead (IRFU9220, SiHFU9220)
- Available in Tape and Reel
- P-Channel
- Fast Switching
- Compliant to RoHS Directive 2002/95/EC



Available

RoHS*
COMPLIANT

DESCRIPTION

Third Power MOSFETs technology is the key to Vishay advanced line of Power MOSFET transistors. The efficient geometry and unique processing of the Power MOSFETs design achieve very low on-state resistance combined with high transconductance and extreme device ruggedness. The DPAK is designed for surface mounting using vapor phase, infrared, or wave soldering techniques. The straight lead version (IRFU, SiHFU series) is for through-hole mounting applications. Power dissipation levels up to 1.5 W are possible in typical surface mount applications.

ORDERING INFORMATION					
Package	DPAK (TO-252)	DPAK (TO-252)	DPAK (TO-252)	DPAK (TO-252)	IPAK (TO-251)
Lead (Pb)-free	IRFR9220PbF	IRFR9220TRLPbF ^a	IRFR9220TRRPbF ^a	IRFR9220TRPbF ^a	IRFU9220PbF
	SiHFR9220-E3	SiHFR9220TL-E3 ^a	SiHFR9220TR-E3 ^a	SiHFR9220T-E3 ^a	SiHFU9220-E3
SnPb	IRFR9220	IRFR9220TRL ^a	IRFR9220TRR ^a	IRFR9220TR ^a	IRFU9220
	SiHFR9220	SiHFR9220TL ^a	SiHFR9220TR ^a	SiHFR9220T ^a	SiHFU9220

Note

a. See device orientation.

ABSOLUTE MAXIMUM RATINGS $T_C = 25$ °C, unless otherwise noted			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	- 200	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current	V_{GS} at - 10 V	$T_C = 25$ °C	- 3.6
		$T_C = 100$ °C	- 2.3
Pulsed Drain Current ^a		I_{DM}	- 14
Linear Derating Factor			0.33
Linear Derating Factor (PCB Mount) ^e			0.020
Single Pulse Avalanche Energy ^b		E_{AS}	310
Repetitive Avalanche Current ^a		I_{AR}	- 3.6
Repetitive Avalanche Energy ^a		E_{AR}	4.2
Maximum Power Dissipation	$T_C = 25$ °C	P_D	42
Maximum Power Dissipation (PCB Mount) ^e	$T_A = 25$ °C		2.5
Peak Diode Recovery dV/dt ^c		dV/dt	- 5.0
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to + 150
Soldering Recommendations (Peak Temperature)			260 ^d

Notes

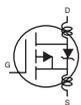
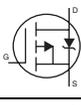
- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = - 50$ V, Starting $T_J = 25$ °C, $L = 35$ mH, $R_g = 25$ Ω , $I_{AS} = - 3.6$ A (see fig. 12).
- $I_{SD} \leq - 3.9$ A, $dI/dt \leq 95$ A/ μ s, $V_{DD} \leq V_{DS}$, $T_J \leq 150$ °C.
- 1.6 mm from case.
- When mounted on 1" square PCB (FR-4 or G-10 material).

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS						
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	
Maximum Junction-to-Ambient	R_{thJA}	-	-	110	°C/W	
Maximum Junction-to-Ambient (PCB Mount) ^a	R_{thJA}	-	-	50		
Maximum Junction-to-Case (Drain)	R_{thJC}	-	-	3.0		

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$		-200	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$, $I_D = -1\text{ mA}$		-	-0.22	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$		-2.0	-	-4.0	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20\text{ V}$		-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -200\text{ V}, V_{GS} = 0\text{ V}$		-	-	-100	μA
		$V_{DS} = -160\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$		-	-	-500	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = -10\text{ V}$	$I_D = -2.2\text{ A}^b$	-	-	1.5	Ω
Forward Transconductance	g_{fs}	$V_{DS} = -50\text{ V}, I_D = -2.2\text{ A}$		1.1	-	-	S
Dynamic							
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = -25\text{ V}, f = 1.0\text{ MHz}$, see fig. 5		-	340	-	pF
Output Capacitance	C_{oss}			-	110	-	
Reverse Transfer Capacitance	C_{rss}			-	33	-	
Total Gate Charge	Q_g	$V_{GS} = -10\text{ V}$	$I_D = -3.9\text{ A}, V_{DS} = -160\text{ V}$, see fig. 6 and 13 ^b	-	-	20	nC
Gate-Source Charge	Q_{gs}			-	-	3.3	
Gate-Drain Charge	Q_{gd}			-	-	11	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -100\text{ V}, I_D = -3.9\text{ A}, R_G = 18\text{ }\Omega, R_D = 24\text{ }\Omega$, see fig. 10 ^b		-	8.8	-	ns
Rise Time	t_r			-	27	-	
Turn-Off Delay Time	$t_{d(off)}$			-	7.3	-	
Fall Time	t_f			-	19	-	
Internal Drain Inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact 		-	4.5	-	nH
Internal Source Inductance	L_S			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p-n junction diode 		-	-	-3.6	A
Pulsed Diode Forward Current ^a	I_{SM}			-	-	-14	
Body Diode Voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}, I_S = -3.6\text{ A}, V_{GS} = 0\text{ V}^b$		-	-	-6.3	V
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}, I_F = -3.9\text{ A}, di/dt = 100\text{ A}/\mu\text{s}^b$		-	150	300	ns
Body Diode Reverse Recovery Charge	Q_{rr}			-	0.97	2.0	μC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

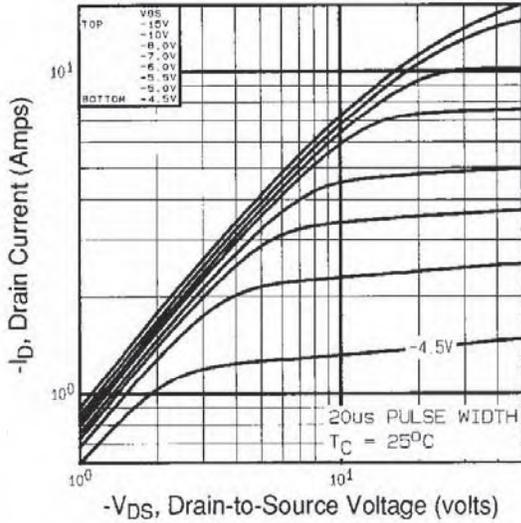


Fig. 1 - Typical Output Characteristics, $T_C = 25\text{ }^\circ\text{C}$

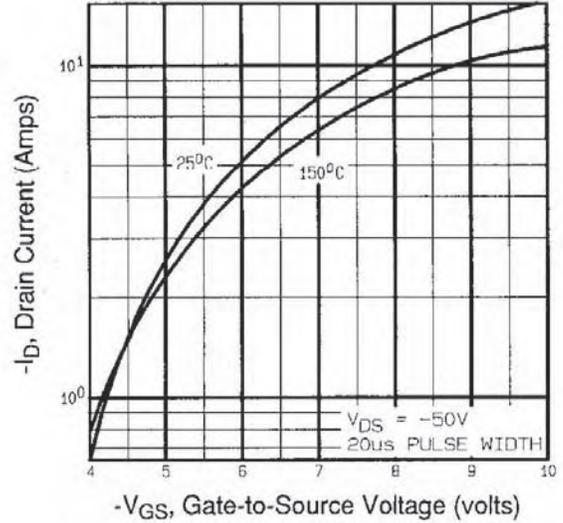


Fig. 3 - Typical Transfer Characteristics

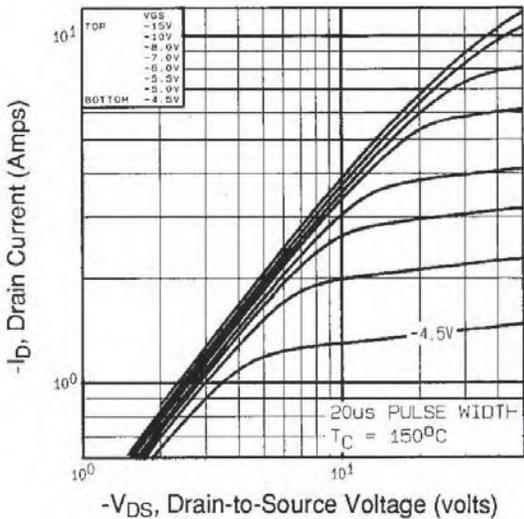


Fig. 2 - Typical Output Characteristics, $T_C = 150\text{ }^\circ\text{C}$

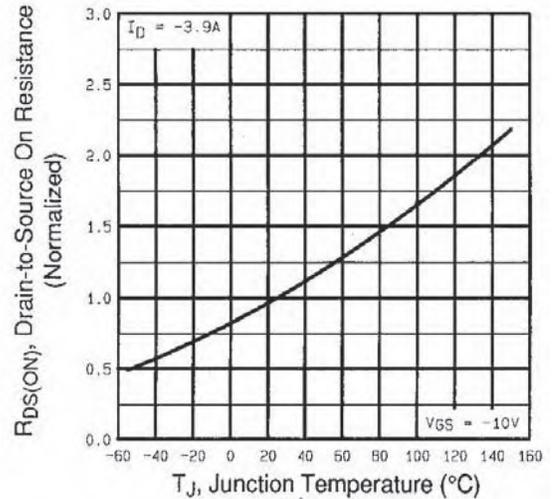


Fig. 4 - Normalized On-Resistance vs. Temperature

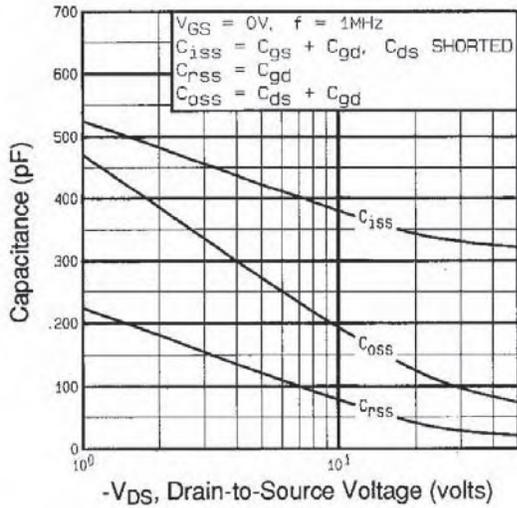


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

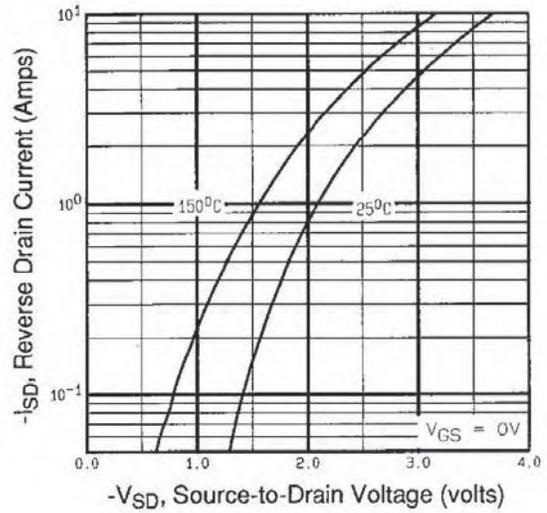


Fig. 7 - Typical Source-Drain Diode Forward Voltage

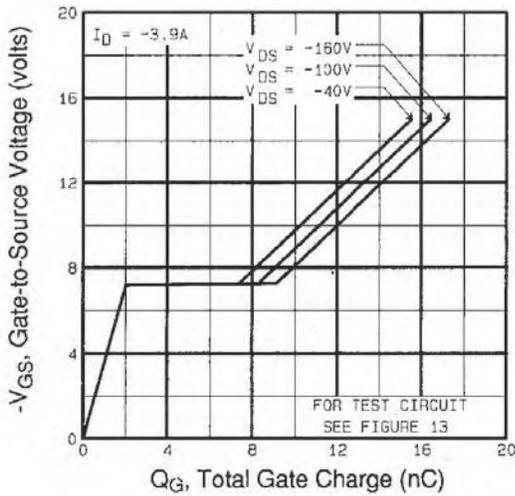


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

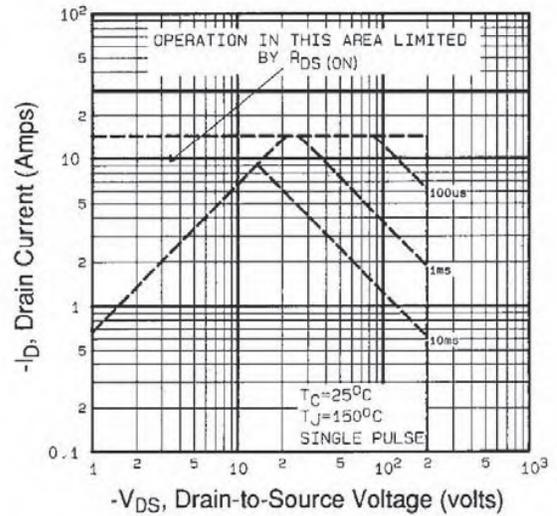


Fig. 8 - Maximum Safe Operating Area

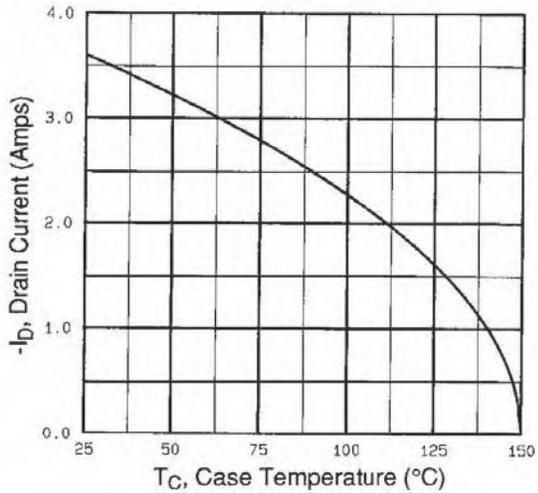


Fig. 9 - Maximum Drain Current vs. Case Temperature

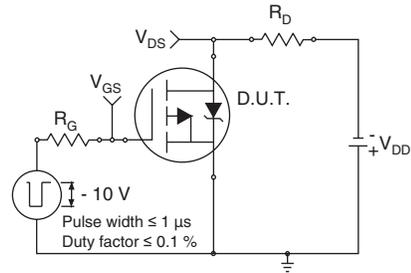


Fig. 10a - Switching Time Test Circuit

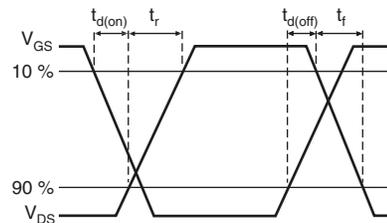


Fig. 10b - Switching Time Waveforms

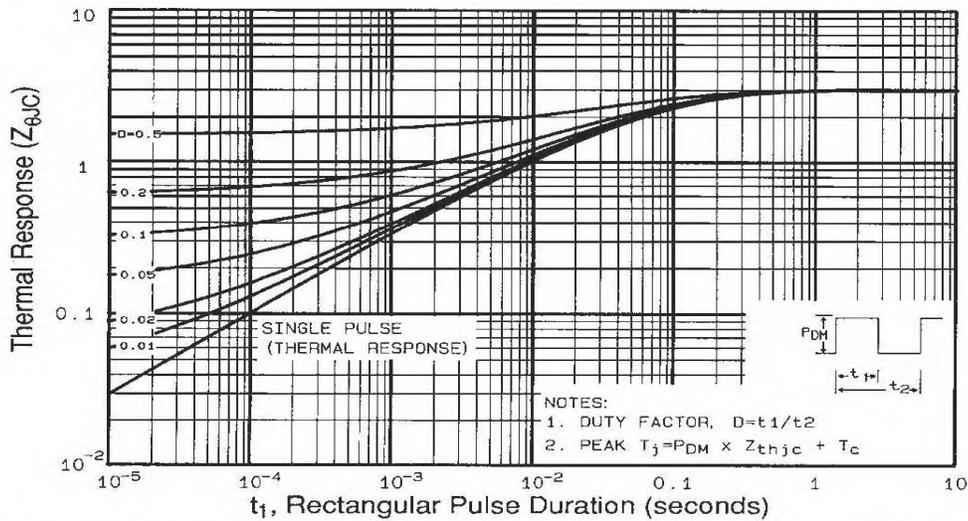


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

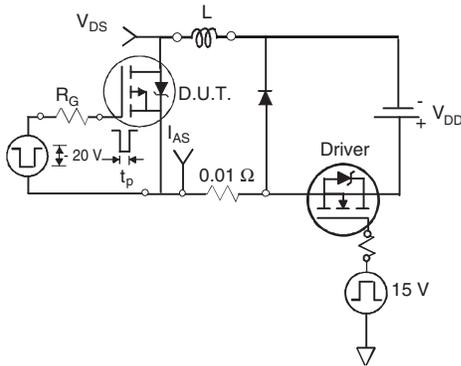


Fig. 12a - Unclamped Inductive Test Circuit

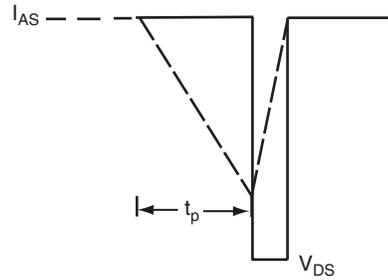


Fig. 12b - Unclamped Inductive Waveforms

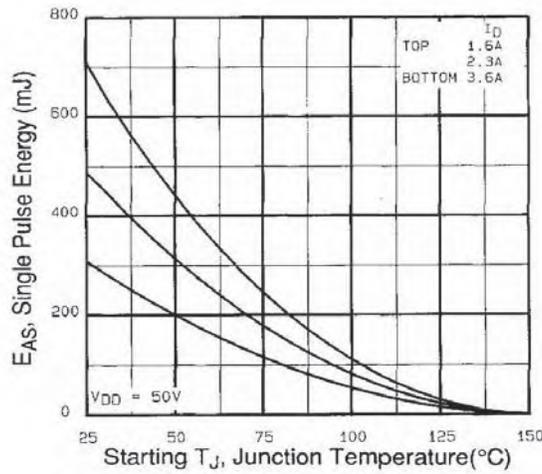


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

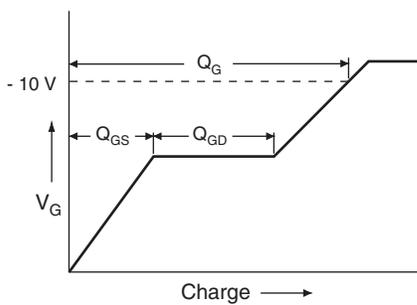


Fig. 13a - Basic Gate Charge Waveform

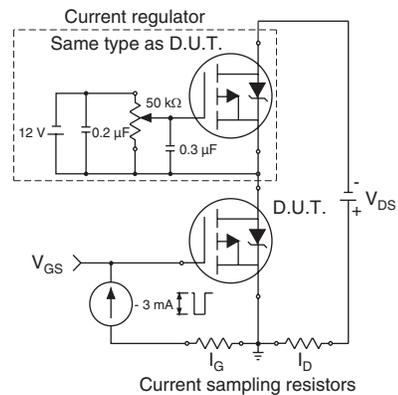
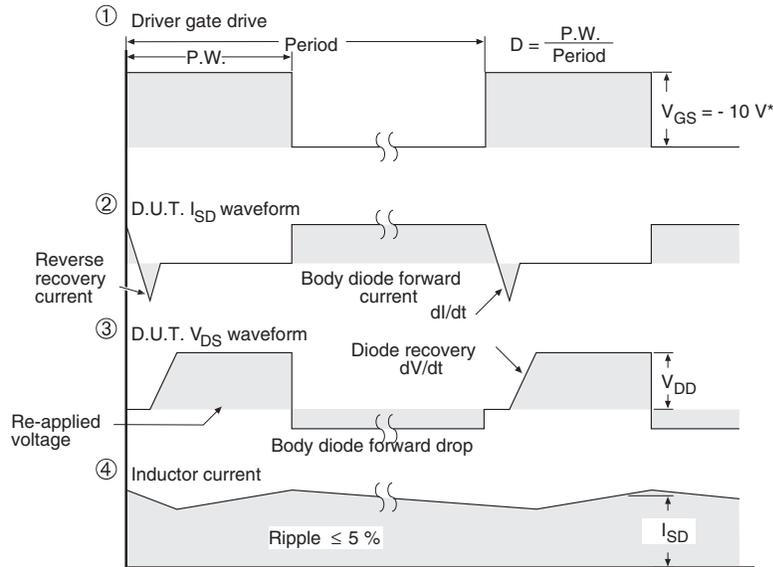
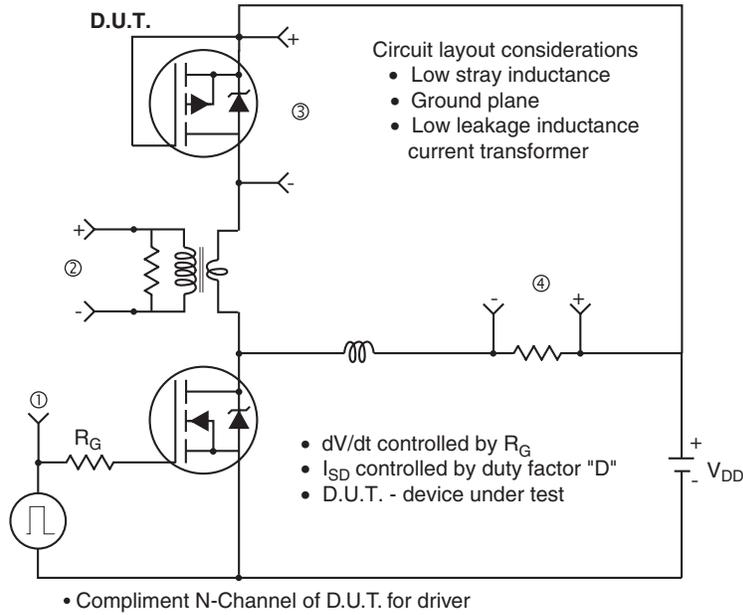


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



* $V_{GS} = -5\text{ V}$ for logic level and -3 V drive devices

Fig. 14 - For P-Channel

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