



Features

- 4A Peak Source/Sink Drive Current
- Wide Operating Voltage Range: 4.5V to 35V
- -40°C to +125°C Extended Operating Temperature Range
- Logic Input Withstands Negative Swing of up to 5V
- Outputs May be Connected in Parallel for Higher Drive Current
- Matched Rise and Fall Times
- Low Propagation Delay Time
- Low, 10µA Supply Current
- Low Output Impedance

Applications

- Efficient Power MOSFET and IGBT Switching
- Switch Mode Power Supplies
- Motor Controls
- DC to DC Converters
- Class-D Switching Amplifiers
- Pulse Transformer Driver



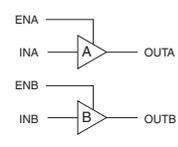
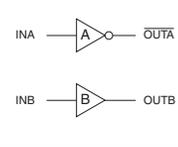
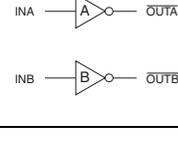
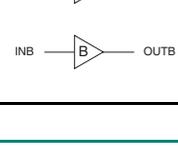
Description

The IXDD604/IXDF604/IXDI604/IXDN604 dual high-speed gate drivers are especially well suited for driving the latest IXYS MOSFETs and IGBTs. Each of the two outputs can source and sink 4A of peak current while producing voltage rise and fall times of less than 10ns. The input of each driver is virtually immune to latch up, and proprietary circuitry eliminates cross conduction and current “shoot-through.” Low propagation delay and fast, matched rise and fall times make the IXD_604 family ideal for high-frequency and high-power applications.

The IXDD604 is a dual non-inverting driver with an enable. The IXDN604 is a dual non-inverting driver, the IXDI604 is a dual inverting driver, and the IXDF604 has one inverting driver and one non-inverting driver.

The IXD_604 family is available in a standard 8-pin DIP (PI), 8-pin SOIC (SIA), 8-pin Power SOIC with an exposed metal back (SI), and an 8-pin DFN (D2) package.

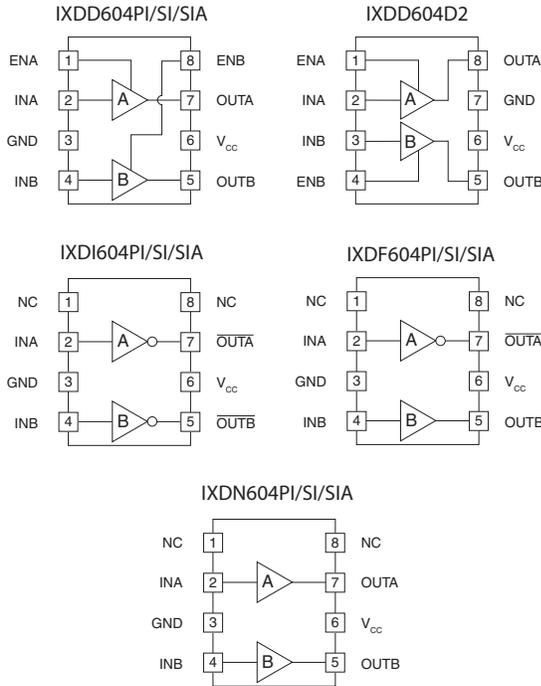
Ordering Information

| Part Number | Logic Configuration | Package Type | Packing Method | Quantity |
|--------------|---|---|----------------|----------|
| IXDD604D2TR |  | 8-Pin DFN | Tape & Reel | 2000 |
| IXDD604PI | | 8-Pin DIP | Tube | 50 |
| IXDD604SI | | 8-Pin Power SOIC with Exposed Metal Back | Tube | 100 |
| IXDD604SITR | | 8-Pin Power SOIC with Exposed Metal Back | Tape & Reel | 2000 |
| IXDD604SIA | | 8-Pin SOIC | Tube | 100 |
| IXDD604SIATR | | 8-Pin SOIC | Tape & Reel | 2000 |
| IXDF604PI |  | 8-Pin DIP | Tube | 50 |
| IXDF604SI | | 8-Pin Power SOIC with Exposed Metal Back | Tube | 100 |
| IXDF604SITR | | 8-Pin Power SOIC with Exposed Metal Back | Tape & Reel | 2000 |
| IXDF604SIA | | 8-Pin SOIC | Tube | 100 |
| IXDF604SIATR | | 8-Pin SOIC | Tape & Reel | 2000 |
| IXDI604PI | |  | 8-Pin DIP | Tube |
| IXDI604SI | 8-Pin Power SOIC with Exposed Metal Back | | Tube | 100 |
| IXDI604SITR | 8-Pin Power SOIC with Exposed Metal Back | | Tape & Reel | 2000 |
| IXDI604SIA | 8-Pin SOIC | | Tube | 100 |
| IXDI604SIATR | 8-Pin SOIC | | Tape & Reel | 2000 |
| IXDN604PI |  | | 8-Pin DIP | Tube |
| IXDN604SI | | 8-Pin Power SOIC with Exposed Metal Back | Tube | 100 |
| IXDN604SITR | | 8-Pin Power SOIC with Exposed Metal Back | Tape & Reel | 2000 |
| IXDN604SIA | | 8-Pin SOIC | Tube | 100 |
| IXDN604SIATR | | 8-Pin SOIC | Tape & Reel | 2000 |

| | |
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1 Specifications

1.1 Pin Configurations



1.2 Pin Definitions

| Pin Name | Description |
|---------------------|--|
| INA | Channel A Logic Input |
| INB | Channel B Logic Input |
| ENA | Channel A Enable Input - Drive pin low to disable Channel A and force Channel A Output to a high impedance state |
| ENB | Channel B Enable Input - Drive pin low to disable Channel B and force Channel B Output to a high impedance state |
| <u>OUTA</u> OUTA | Channel A Output - Sources or sinks current to turn-on or turn-off a discrete MOSFET or IGBT |
| <u>OUTB</u> OUTB | Channel B Output - Sources or sinks current to turn-on or turn-off a discrete MOSFET or IGBT |
| V _{CC} | Supply Voltage - Provides power to the device |
| GND | Ground - Common ground reference for the device |

1.3 Absolute Maximum Ratings

| Parameter | Symbol | Minimum | Maximum | Units |
|----------------------|-------------------------------------|---------|----------------------|-------|
| Supply Voltage | V _{CC} | -0.3 | 40 | V |
| Input Voltage | V _{INX} , V _{ENX} | -5 | V _{CC} +0.3 | V |
| Output Current | I _{OUT} | - | ±4 | A |
| Junction Temperature | T _J | -55 | +150 | °C |
| Storage Temperature | T _{STG} | -65 | +150 | °C |

Absolute maximum electrical ratings are at 25°C

Absolute maximum ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at conditions beyond those indicated in the operational sections of this data sheet is not implied.

1.4 Recommended Operating Conditions

| Parameter | Symbol | Range | Units |
|-----------------------------|-----------------|-------------|-------|
| Supply Voltage | V _{CC} | 4.5 to 35 | V |
| Operating Temperature Range | T _A | -40 to +125 | °C |

1.5 Electrical Characteristics: $T_A = 25^\circ\text{C}$

 Test Conditions: $4.5\text{V} \leq V_{CC} \leq 35\text{V}$, one channel (unless otherwise noted).

| Parameter | Conditions | Symbol | Minimum | Typical | Maximum | Units | |
|--|---|--------------|----------------|---------|-------------|---------------|------------------|
| Input Voltage, High | $4.5\text{V} \leq V_{CC} \leq 18\text{V}$ | V_{IH} | 3.0 | - | - | V | |
| Input Voltage, Low | $4.5\text{V} \leq V_{CC} \leq 18\text{V}$ | V_{IL} | - | - | 0.8 | | |
| Input Current | $0\text{V} \leq V_{IN} \leq V_{CC}$ | I_{IN} | - | - | ± 10 | μA | |
| High EN Input Voltage | IXDD604 only | V_{ENH} | $2/3V_{CC}$ | - | - | V | |
| Low EN Input Voltage | IXDD604 only | V_{ENL} | - | - | $1/3V_{CC}$ | | |
| Output Voltage, High | - | V_{OH} | $V_{CC}-0.025$ | - | - | V | |
| Output Voltage, Low | - | V_{OL} | - | - | 0.025 | | |
| Output Resistance, High State | $V_{CC}=18\text{V}, I_{OUT}=-10\text{mA}$ | R_{OH} | - | 1.3 | 2.5 | Ω | |
| Output Resistance, Low State | $V_{CC}=18\text{V}, I_{OUT}=10\text{mA}$ | R_{OL} | - | 1.1 | 2 | | |
| Output Current, Continuous | Limited by package power dissipation | I_{DC} | - | - | ± 1 | A | |
| Rise Time | $V_{CC}=18\text{V}, C_{LOAD}=1000\text{pF}$ | t_r | - | 9 | 16 | ns | |
| Fall Time | $V_{CC}=18\text{V}, C_{LOAD}=1000\text{pF}$ | t_f | - | 8 | 14 | | |
| On-Time Propagation Delay | $V_{CC}=18\text{V}, C_{LOAD}=1000\text{pF}$ | t_{ondly} | - | 29 | 50 | | |
| Off-Time Propagation Delay | $V_{CC}=18\text{V}, C_{LOAD}=1000\text{pF}$ | t_{offdly} | - | 35 | 50 | | |
| Enable to Output-High Delay Time | IXDD604 only, $V_{CC}=18\text{V}$ | t_{ENOH} | - | 35 | 55 | | |
| Disable to High Impedance State Delay Time | IXDD604 only, $V_{CC}=18\text{V}$ | t_{DOLD} | - | 40 | 55 | | |
| Enable Pull-Up Resistor | - | R_{EN} | - | 200 | - | | $\text{k}\Omega$ |
| Power Supply Current | $V_{CC}=18\text{V}, V_{IN}=3.5\text{V}$ | I_{CC} | - | 1 | 3 | | mA |
| | $V_{CC}=18\text{V}, V_{IN}=0\text{V}$ | | - | <1 | 10 | | |
| | $V_{CC}=18\text{V}, V_{IN}=V_{CC}$ | | - | <1 | 10 | μA | |

1.6 Electrical Characteristics: $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$

 Test Conditions: $4.5\text{V} \leq V_{CC} \leq 35\text{V}$, one channel (unless otherwise noted).

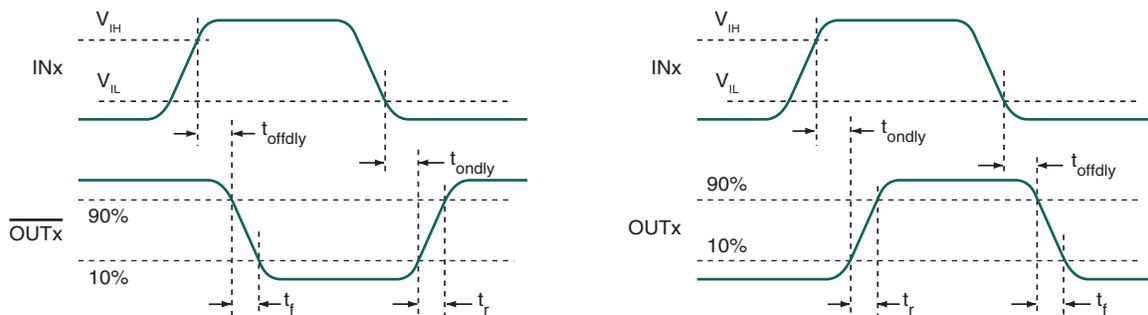
| Parameter | Conditions | Symbol | Minimum | Maximum | Units | |
|--|---|--------------|----------------|---------|---------------|----|
| Input Voltage, High | $4.5\text{V} \leq V_{CC} \leq 18\text{V}$ | V_{IH} | 3.1 | - | V | |
| Input Voltage, Low | $4.5\text{V} \leq V_{CC} \leq 18\text{V}$ | V_{IL} | - | 0.65 | | |
| Input Current | $0\text{V} \leq V_{IN} \leq V_{CC}$ | I_{IN} | -10 | 10 | μA | |
| Output Voltage, High | - | V_{OH} | $V_{CC}-0.025$ | - | V | |
| Output Voltage, Low | - | V_{OL} | - | 0.025 | | |
| Output Resistance, High State | $V_{CC}=18\text{V}, I_{OUT}=-10\text{mA}$ | R_{OH} | - | 3 | Ω | |
| Output Resistance, Low State | $V_{CC}=18\text{V}, I_{OUT}=10\text{mA}$ | R_{OL} | - | 2.5 | | |
| Output Current, Continuous | Limited by package power dissipation | I_{DC} | - | ± 1 | A | |
| Rise Time | $V_{CC}=18\text{V}, C_{LOAD}=1000\text{pF}$ | t_r | - | 16 | ns | |
| Fall Time | $V_{CC}=18\text{V}, C_{LOAD}=1000\text{pF}$ | t_f | - | 14 | | |
| On-Time Propagation Delay | $V_{CC}=18\text{V}, C_{LOAD}=1000\text{pF}$ | t_{ondly} | - | 65 | | |
| Off-Time Propagation Delay | $V_{CC}=18\text{V}, C_{LOAD}=1000\text{pF}$ | t_{offdly} | - | 65 | | |
| Enable to Output-High Delay Time | IXDD604 only, $V_{CC}=18\text{V}$ | t_{ENOH} | - | 65 | | |
| Disable to High Impedance State Delay Time | IXDD604 only, $V_{CC}=18\text{V}$ | t_{DOLD} | - | 65 | | |
| Power Supply Current | $V_{CC}=18\text{V}, V_{IN}=3.5\text{V}$ | I_{CC} | - | 3.5 | | mA |
| | $V_{CC}=18\text{V}, V_{IN}=0\text{V}$ | | - | 150 | | |
| | $V_{CC}=18\text{V}, V_{IN}=V_{CC}$ | | - | 150 | μA | |

1.7 Thermal Characteristics

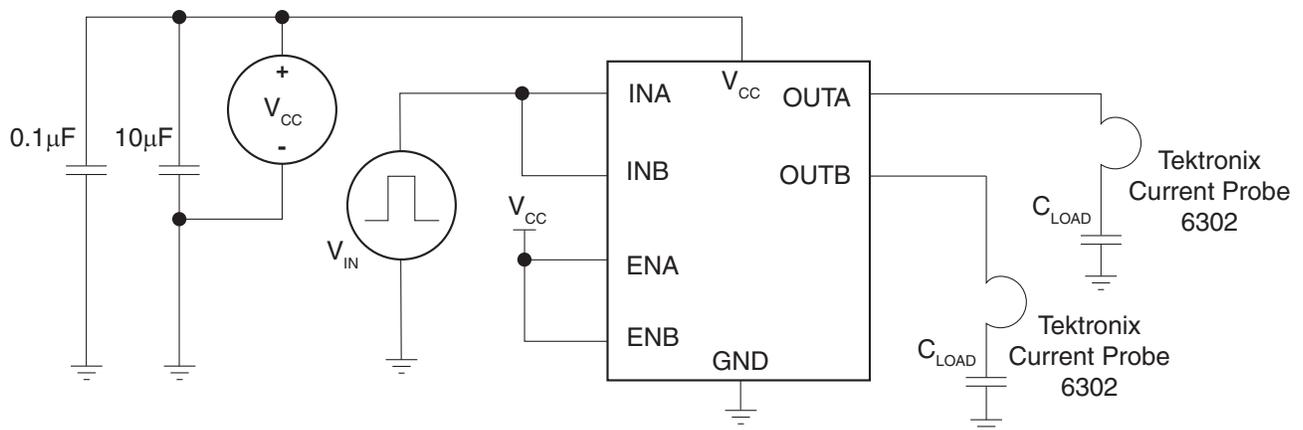
| Package | Parameter | Symbol | Rating | Units |
|-----------------------|---|---------------|--------|-------|
| D2 (8-Pin DFN) | Thermal Resistance, Junction-to-Ambient | θ_{JA} | 35 | °C/W |
| PI (8-Pin DIP) | | | 125 | |
| SI (8-Pin Power SOIC) | | | 85 | |
| SIA (8-Pin SOIC) | | | 120 | |
| SI (8-Pin Power SOIC) | Thermal Resistance, Junction-to-Case | θ_{JC} | 10 | °C/W |

2 IXD_604 Performance

2.1 Timing Diagrams

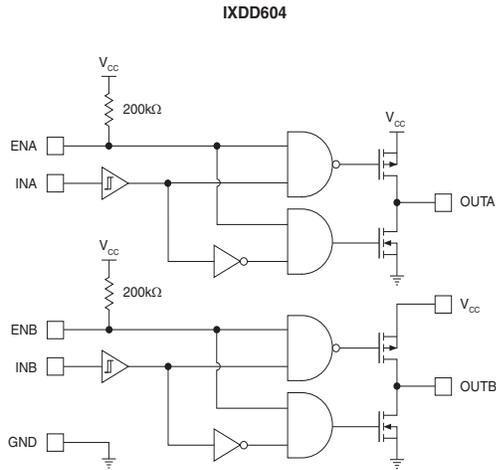


2.2 Characteristics Test Diagram



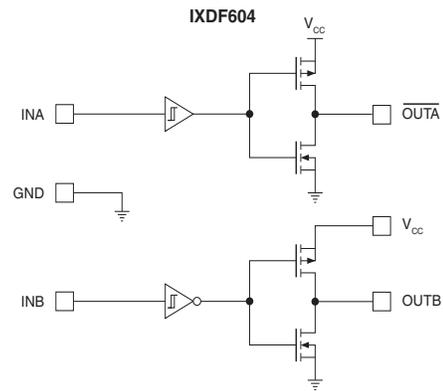
3 Block Diagrams & Truth Tables

3.1 IXDD604



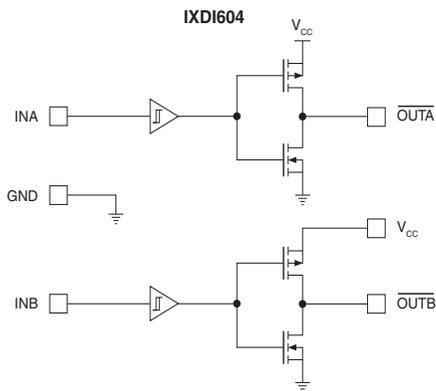
| IN _x | EN _x | OUT _x |
|-----------------|-----------------|------------------|
| 0 | 1 or open | 0 |
| 1 | 1 or open | 1 |
| 0 | 0 | Z |
| 1 | 0 | Z |

3.3 IXDF604



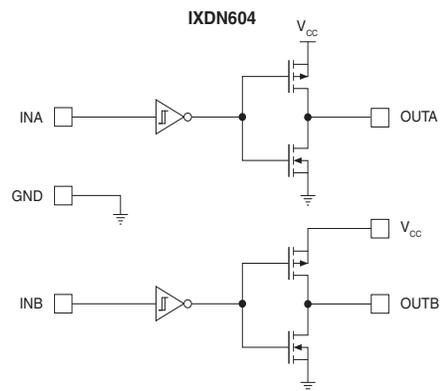
| INA | $\overline{\text{OUTA}}$ |
|-----|--------------------------|
| 0 | 1 |
| 1 | 0 |
| INB | OUTB |
| 0 | 0 |
| 1 | 1 |

3.2 IXDI604



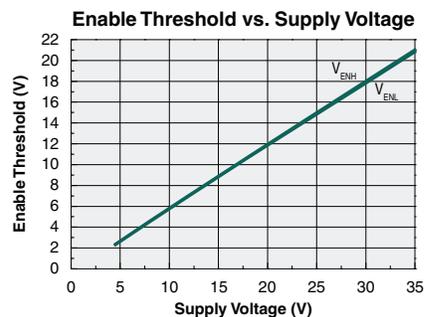
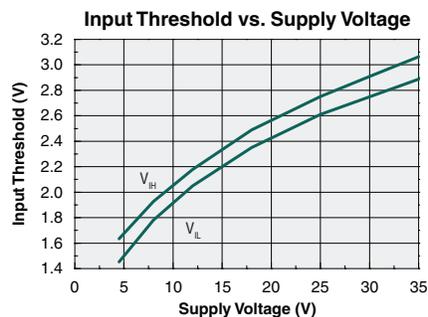
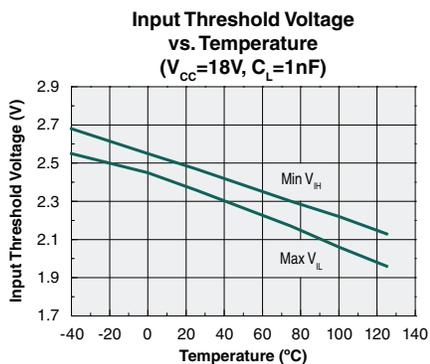
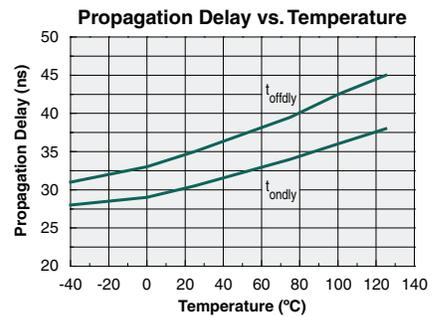
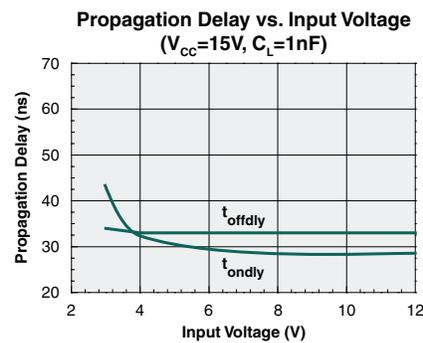
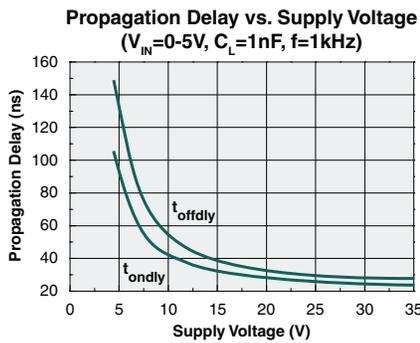
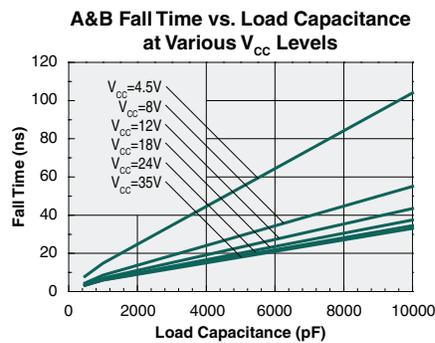
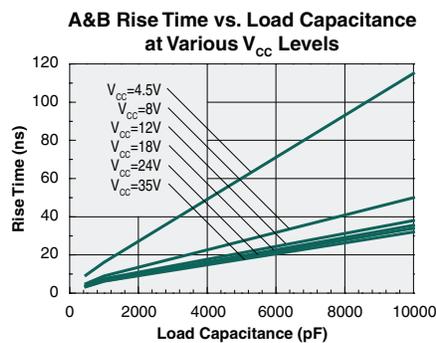
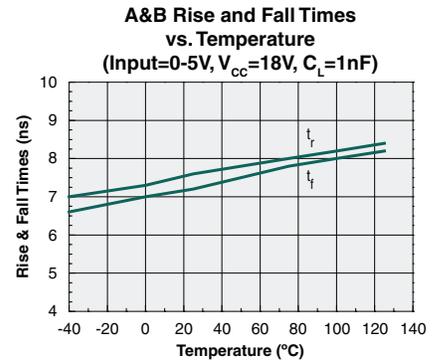
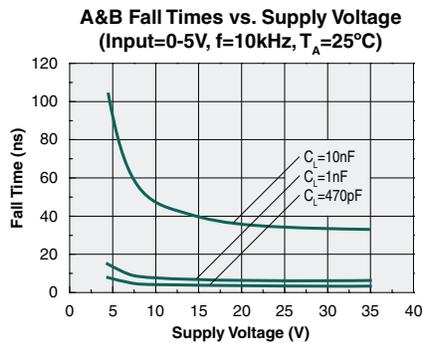
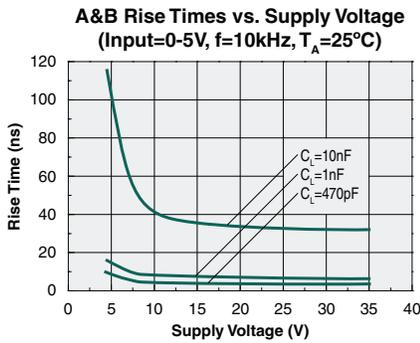
| IN _x | $\overline{\text{OUT}}_x$ |
|-----------------|---------------------------|
| 0 | 1 |
| 1 | 0 |

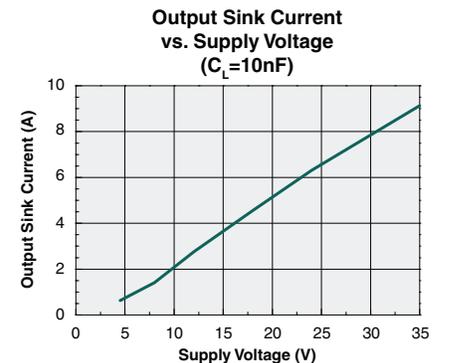
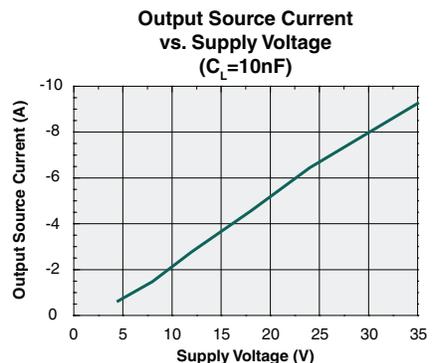
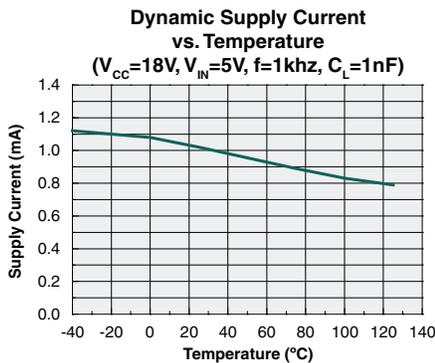
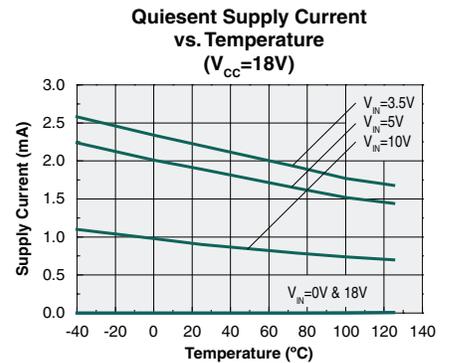
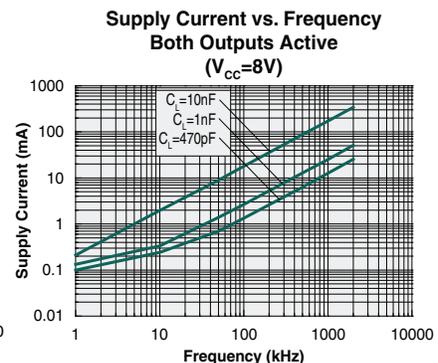
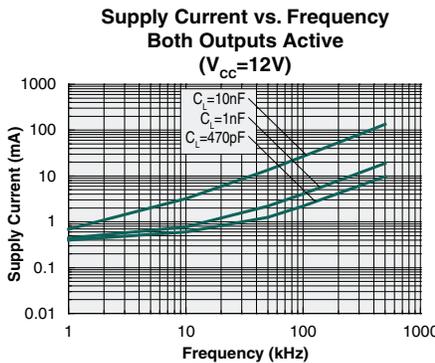
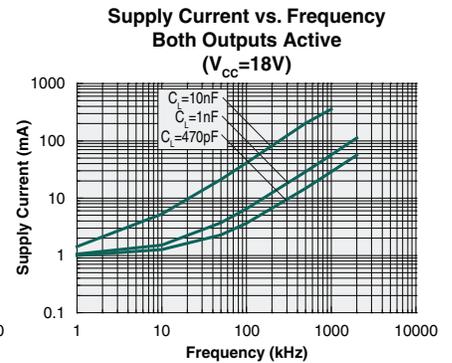
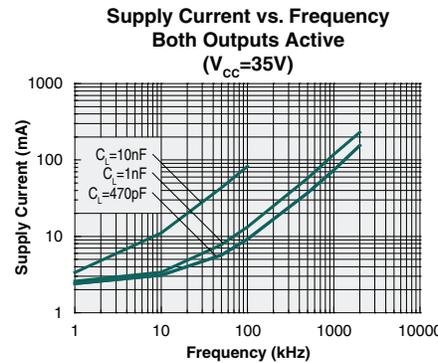
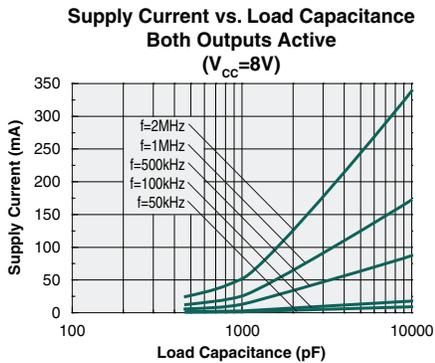
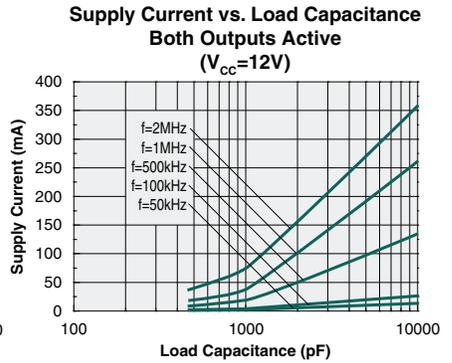
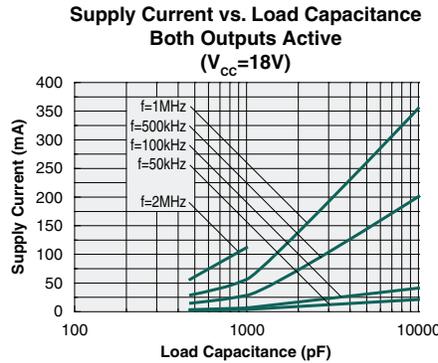
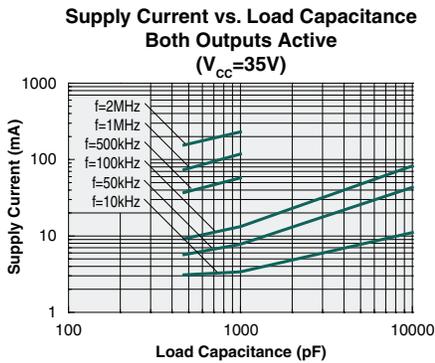
3.4 IXDN604

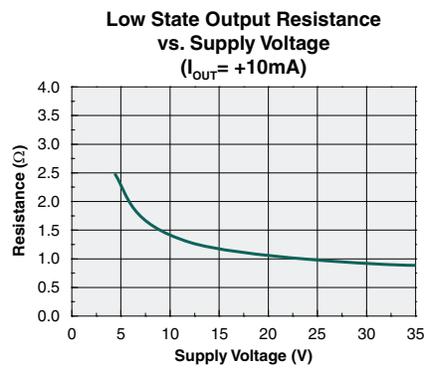
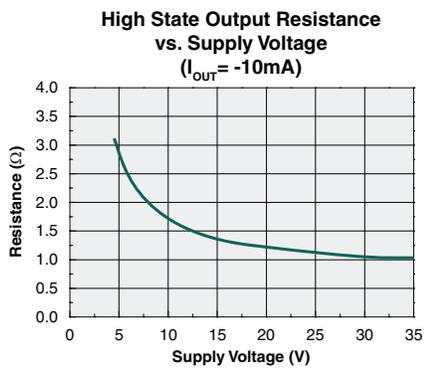
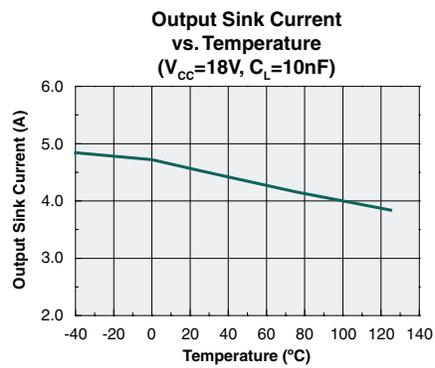
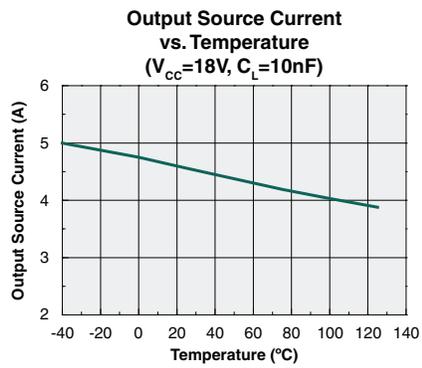


| IN _x | OUT _x |
|-----------------|------------------|
| 0 | 0 |
| 1 | 1 |

4 Typical Performance Characteristics







5 Manufacturing Information

5.1 Moisture Sensitivity



All plastic encapsulated semiconductor packages are susceptible to moisture ingress. IXYS Integrated Circuits Division classified all of its plastic encapsulated devices for moisture sensitivity according to the latest version of the joint industry standard, **IPC/JEDEC J-STD-020**, in force at the time of product evaluation. We test all of our products to the maximum conditions set forth in the standard, and guarantee proper operation of our devices when handled according to the limitations and information in that standard as well as to any limitations set forth in the information or standards referenced below.

Failure to adhere to the warnings or limitations as established by the listed specifications could result in reduced product performance, reduction of operable life, and/or reduction of overall reliability.

This product carries a **Moisture Sensitivity Level (MSL) rating** as shown below, and should be handled according to the requirements of the latest version of the joint industry standard **IPC/JEDEC J-STD-033**.

| Device | Moisture Sensitivity Level (MSL) Rating |
|------------------------------------|---|
| IXD_604SI / IXD_604SIA / IXD_604PI | MSL 1 |
| IXD_604D2 | MSL 3 |

5.2 ESD Sensitivity



This product is **ESD Sensitive**, and should be handled according to the industry standard **JESD-625**.

5.3 Reflow Profile

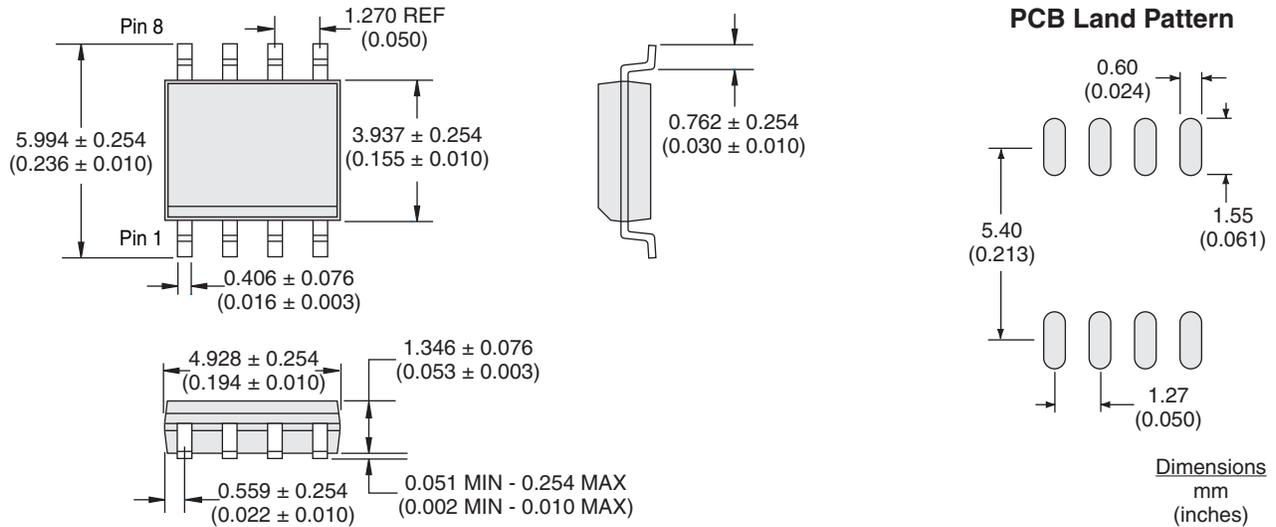
This product has a maximum body temperature and time rating as shown below. All other guidelines of **J-STD-020** must be observed.

| Device | Maximum Temperature x Time |
|------------------------------------|----------------------------|
| IXD_604SI / IXD_604SIA / IXD_604D2 | 260°C for 30 seconds |
| IXD_604PI | 250°C for 30 seconds |

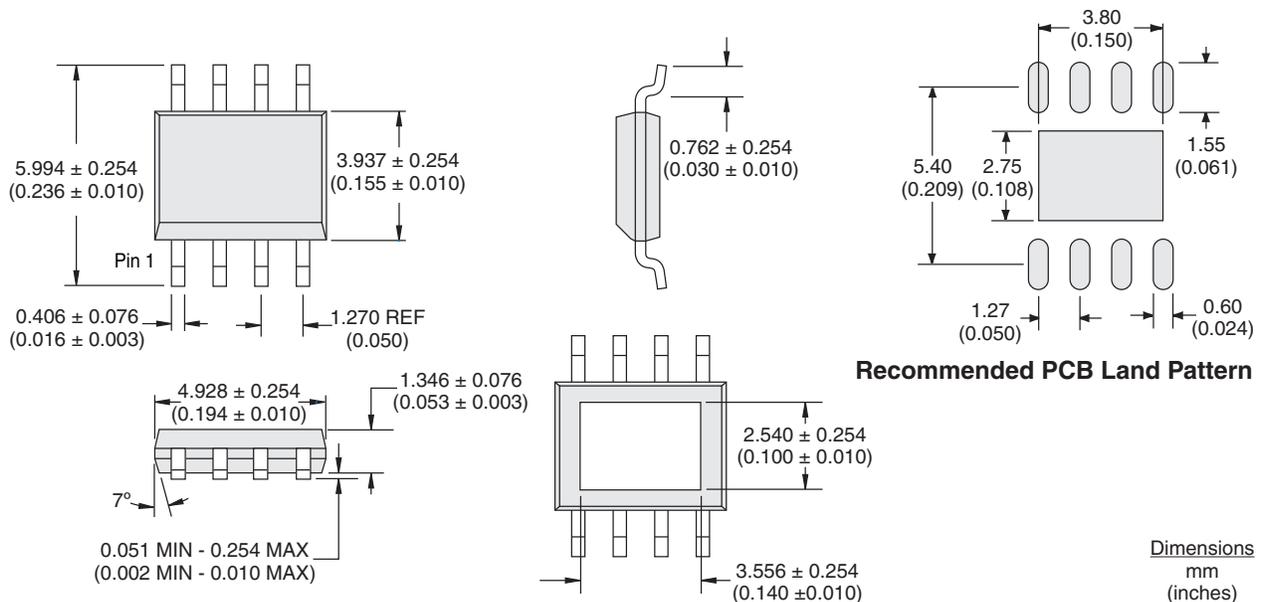


5.4 Mechanical Dimensions

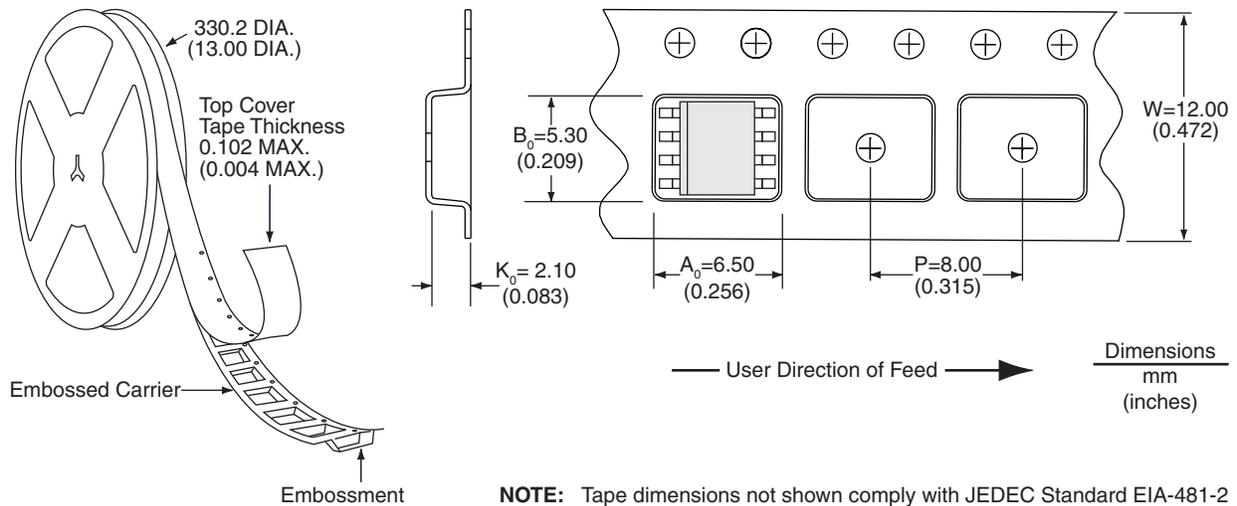
5.4.1 SIA (8-Pin SOIC)



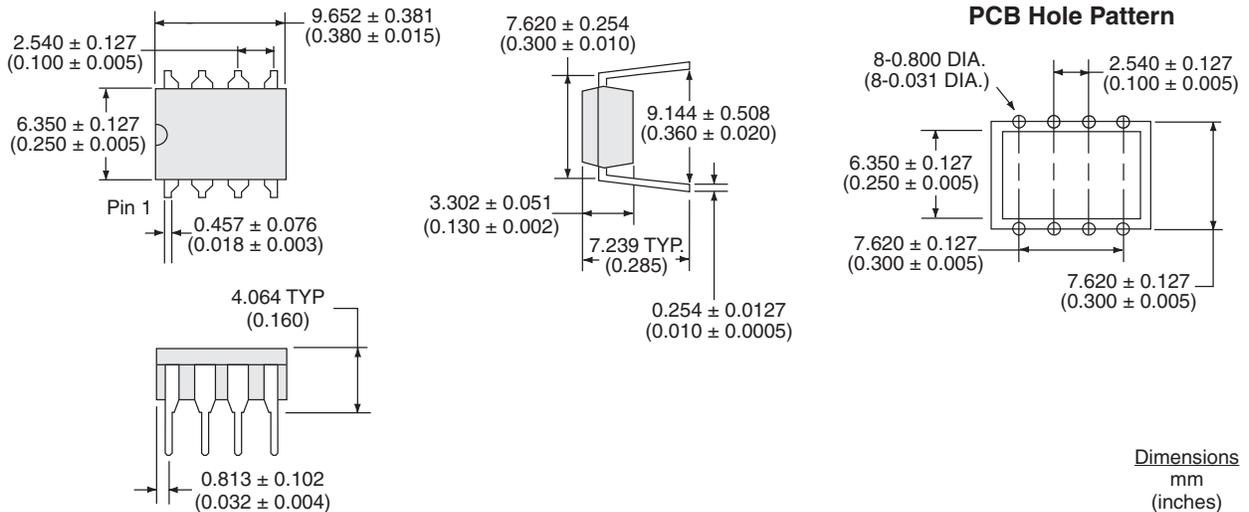
5.4.2 SI (8-Pin Power SOIC with Exposed Metal Back)



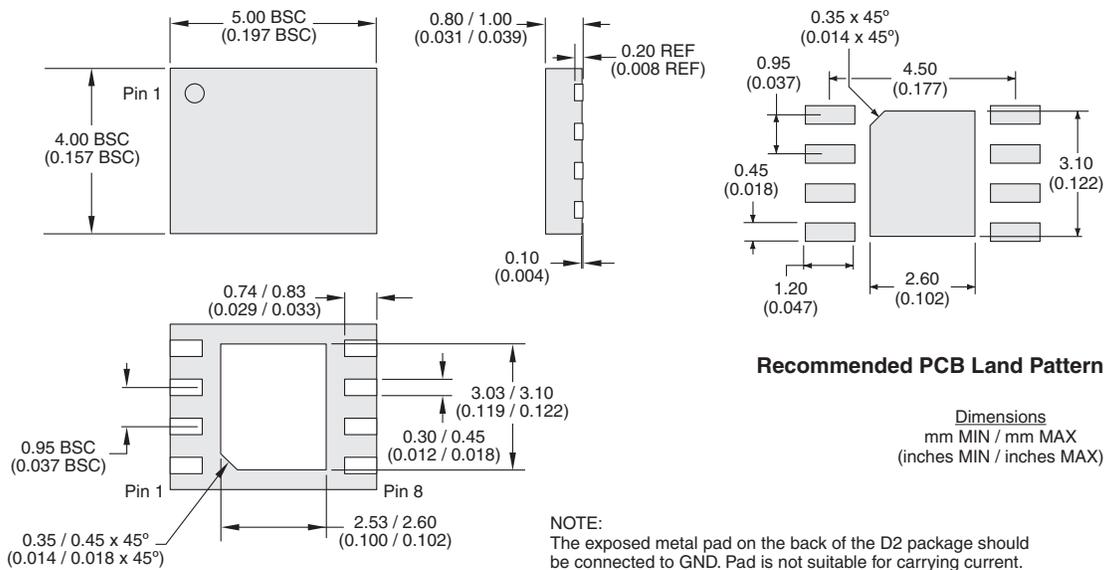
5.4.3 Tape & Reel Information for SI and SIA Packages



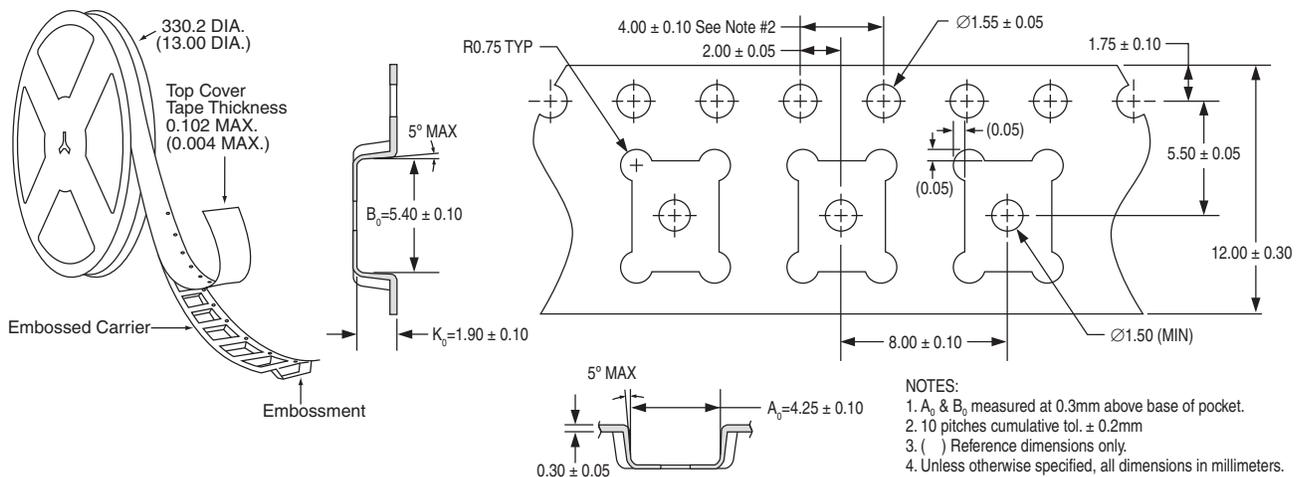
5.4.4 PI (8-Pin DIP)



5.4.5 D2 (8-Pin DFN)



5.4.6 Tape & Reel Information for D2 Package



For additional information please visit our website at: www.ixysic.com

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