| Product Specification<br>Type Number : M T M C 8 E 2 A 0 L B F *1) | Prepared by S.Miyata | Checked by M.Fujisawa | Applied by K.Hagi | Established by H. Shidouka |
|---|---|---|---|---|

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Type | Silicon Field Effect Transistors | | | | | | | | |
| Application | Li-ion Battery | | | | | | | | |
| Structure | Gate Resistor installed Dual N-Channel MOS Type | | | | | | | | |
| Outline | WMini8 - F1 | | | | | | Marking | | 4B |
| Absolute Maximum Ratings | VDSS | VGSS | ID | IDp | *2) PD1 | *2,*3) PD2 | *4) PD3 | Tch | Tstg |
| | 20 (V) | ±12 (V) | 7.0 (A) | 42 (A) | 1.0 (W) | 1.2 (W) | 0.4 (W) | 150 (°C) | -55 to +150 (°C) |

Electrical characteristics (Ta = 25 °C ±3 °C)

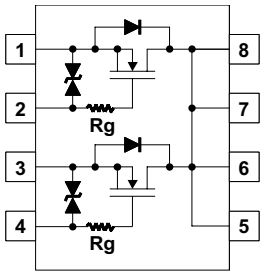
| Item | Symbol | Measuring condition | Limit min. | Limit typ. | Limit max. | Unit |
|---|---|---|---|---|---|---|
| Drain-Source Voltage | VDSS | ID = 1.0 mA, VGS = 0 V | 20 | | | V |
| Drain-Source Cutoff Current | IDSS | VDS = 20 V, VGS = 0 V | | | 1.0 | μA |
| Gate-Source Cutoff Current | IGSS | VGS = ±8.0 V, VDS = 0 V | | | ±10 | μA |
| Gate Threshold Voltage | Vth | ID = 1.0 mA, VDS = 10 V | 0.40 | 0.85 | 1.3 | V |
| Drain Resistance (ON) 1 | RDS(ON) 1 | ID = 2.0 A, VGS = 4.5 V | | 15 | 21 | mΩ |
| Drain Resistance (ON) 2 | RDS(ON) 2 | ID = 2.0 A, VGS = 3.7 V | | 18 | 25 | mΩ |
| Drain Resistance (ON) 3 | RDS(ON) 3 | ID = 2.0 A, VGS = 2.5 V | | 22 | 33 | mΩ |
| Forward Transfer Admittance | \|Yfs\| | ID = 1.0 A, VDS = 10 V | 3.0 | | | S |
| Small-Signal Short-Circuit Input Capacitance | Ciss | VDS = 10 V, VGS = 0 V, f = 1 MHz | | 1450 | | pF |
| Small-Signal Short-Circuit Output Capacitance | Coss | VDS = 10 V, VGS = 0 V, f = 1 MHz | | 100 | | pF |
| Small-Signal Reverse Transfer Capacitance | Crss | VDS = 10 V, VGS = 0 V, f = 1 MHz | | 90 | | pF |
| Turn-on Delay Time | td(on) *5) | VDD = 10 V, VGS = 0 to 4 V, ID = 1.0 A | | 0.33 | | μs |
| Rise Time | tr *5) | VDD = 10 V, VGS = 0 to 4 V, ID = 1.0 A | | 0.70 | | μs |
| Turn-off Delay Time | td(off) *5) | VDD = 10 V, VGS = 4 to 0 V, ID = 1.0 A | | 4.0 | | μs |
| Fall Time | tf *5) | VDD = 10 V, VGS = 4 to 0 V, ID = 1.0 A | | 2.0 | | μs |

Note: Measuring methods for transistors are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030.

*1 Packing: Embossed TX Type (Thermo-compression sealing)
*2 Glass epoxy board (25.4 x 25.4 x t0.8 mm) coated with copper foil, which has more than 300mm$^2$.
*3 t = 10 s
*4 Stand-alone (without the board)
*5 Refer to test circuit

Internally connected circuit

1.Source1
2.Gate1
3.Source2
4.Gate2
5.Drain
6.Drain
7.Drain
8.Drain

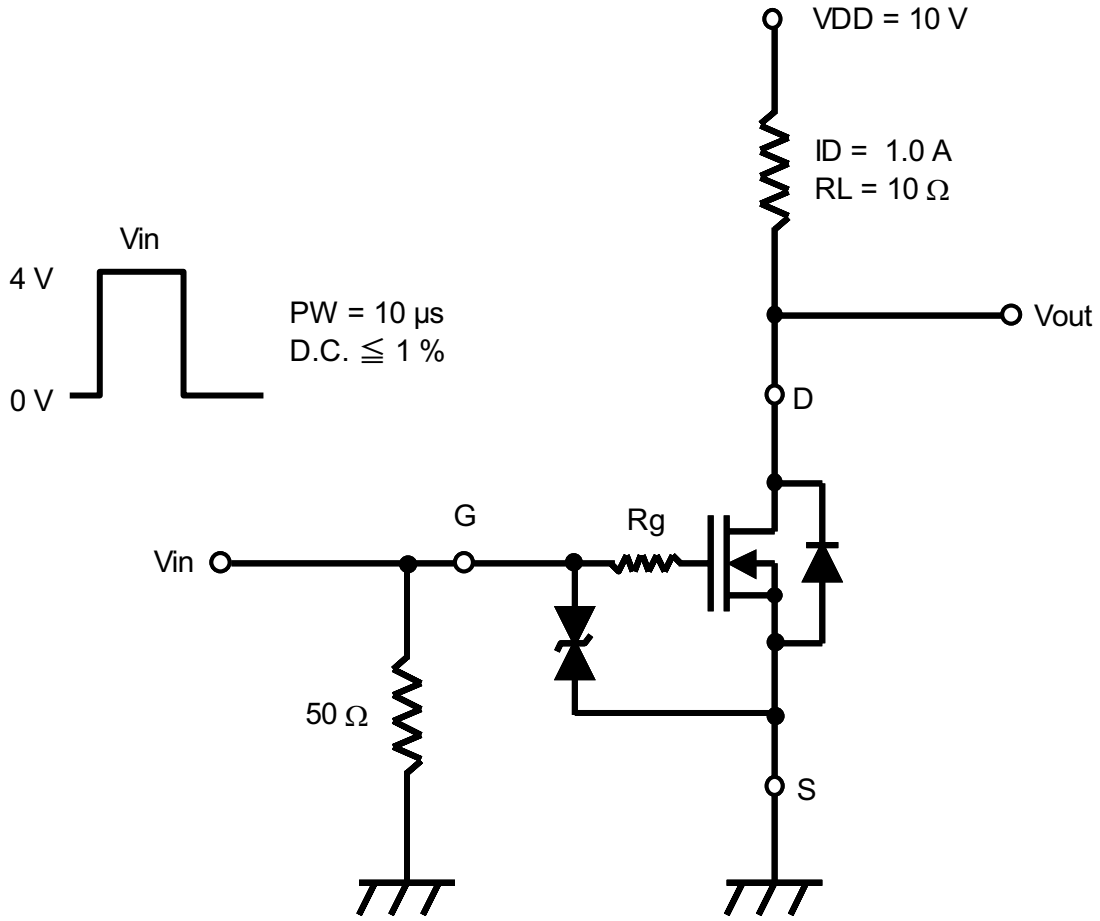


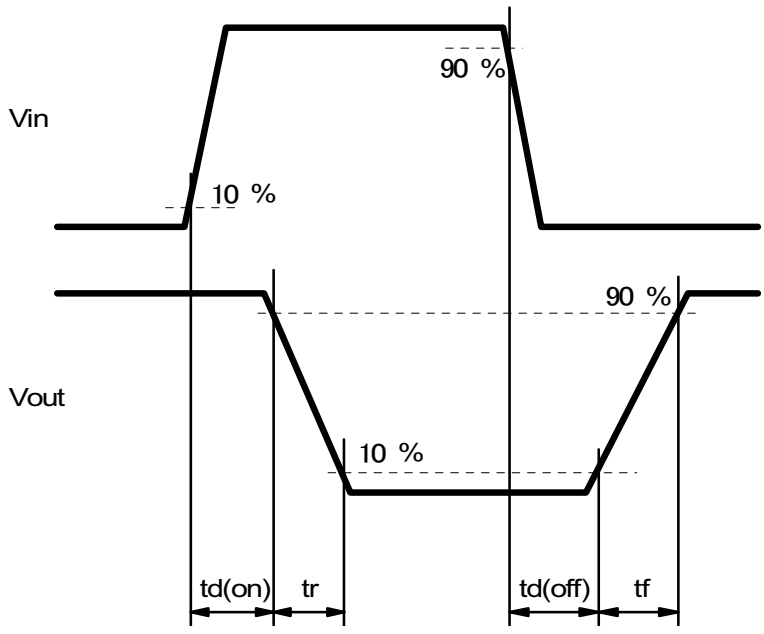

Rg = 1kΩ

| 2009.04.08 | |
|---|---|
| Established | Revised |

| Product Specification<br>Type Number : M T M C 8 E 2 A 0 L B F *1) | |
|---|---|

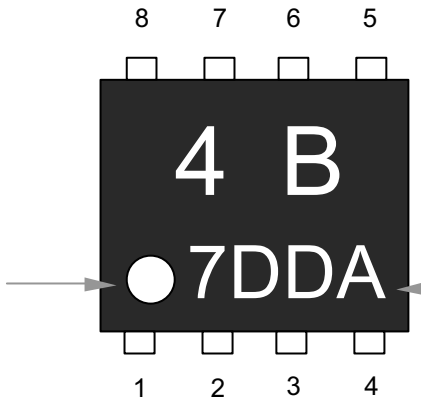
Test circuit




| 2009.04.08 | |
|---|---|
| Established | Revised |

Product Specification
Mark Indication
Type Number : M T M C 8 E 2 A 0 [L] B F
*1)




Indication of No.1 lead

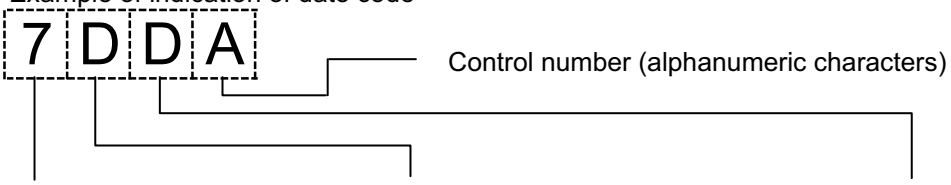
Indication of date code

Connection

| | |
|---|---|
| 1.Source1 | 5.Drain |
| 2.Gate1 | 6.Drain |
| 3.Source2 | 7.Drain |
| 4.Gate2 | 8.Drain |

The actual font of product symbol may differ slightly from the font shown in this specification.

<<Example of indication of date code>>

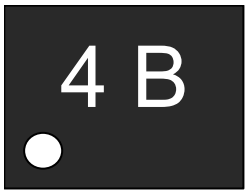
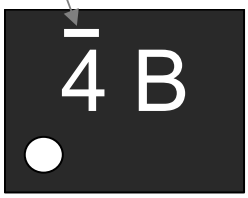



AD2007 → 7
AD2008 → 8
AD2009 → 9
AD2010 → 0

Jan. to Sep. → 1 to 9
Oct. → O
Nov. → N
Dec. → D

| Day | Symbol | Day | Symbol | Day | Symbol |
|---|---|---|---|---|---|
| 1 | 1 | 11 | A | 21 | M |
| 2 | 2 | 12 | B | 22 | N |
| 3 | 3 | 13 | C | 23 | P |
| 4 | 4 | 14 | D | 24 | R |
| 5 | 5 | 15 | E | 25 | S |
| 6 | 6 | 16 | F | 26 | T |
| 7 | 7 | 17 | H | 27 | U |
| 8 | 8 | 18 | J | 28 | V |
| 9 | 9 | 19 | K | 29 | W |
| 10 | 0 | 20 | L | 30 | X |
| | | | | 31 | Y |

・Factory distinction mark

| Factory | JAPAN | CHINA |
|---|---|---|
| Package code | WMini8 - F1 | WMini8 - F1 |
| Marking | No distinction mark  | CHINA  |



※White parts are treated by laser mark.

| 2009.04.08 | |
|---|---|
| Established | Revised |

# PACKAGE STANDARDS

| Package Code | WMini8-F1 |
|---|---|

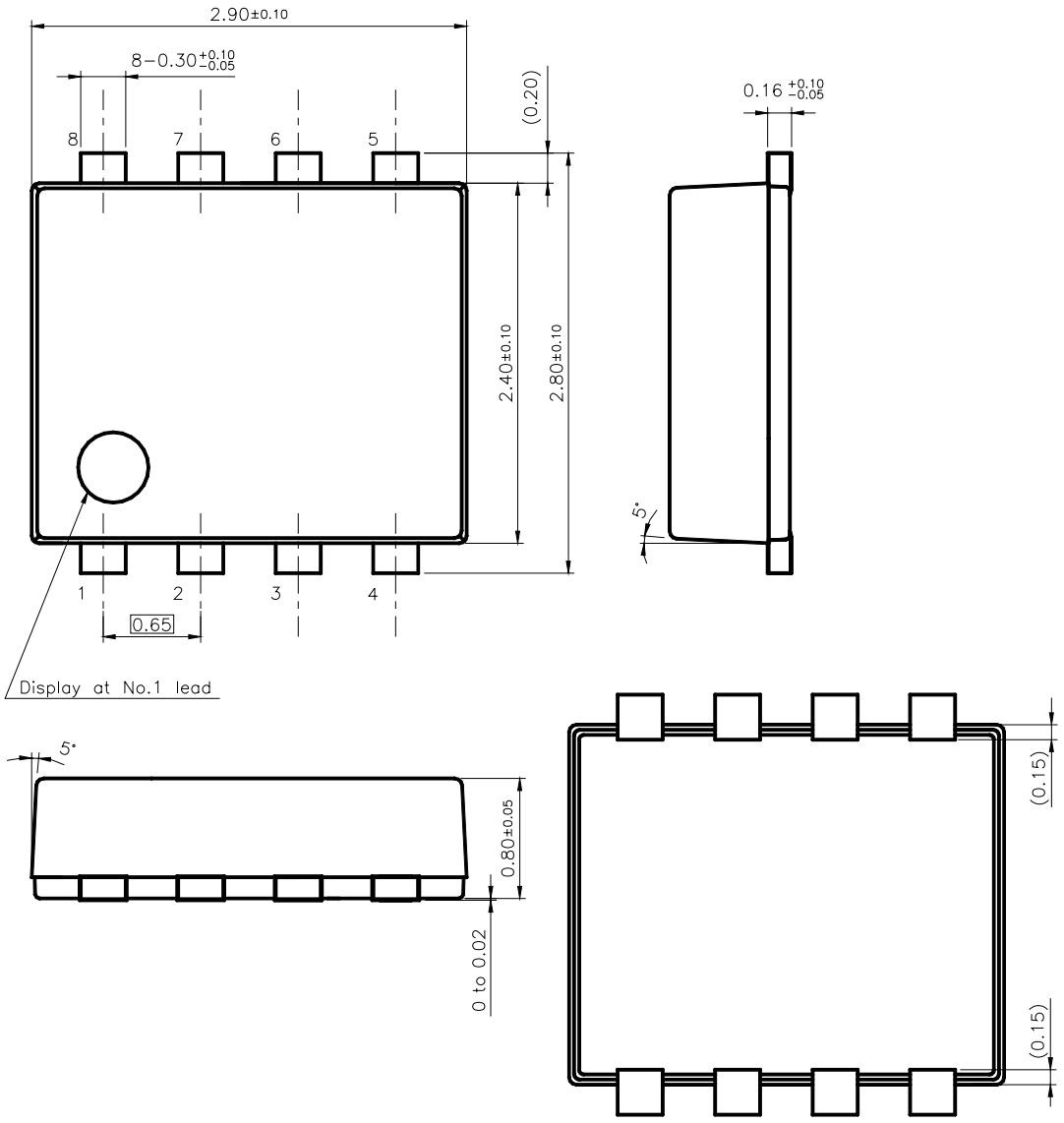
Semiconductor Company
Panasonic Corporation

| Established by | Applied by | Checked by | Prepared by |
|---|---|---|---|
| H.Shidooka | H.Yoshida | M.Okajima | M.Kametaka |


Established: 2006-09-01
Revised : 2009-01-29

## 1. Outline Drawing

Unit:mm

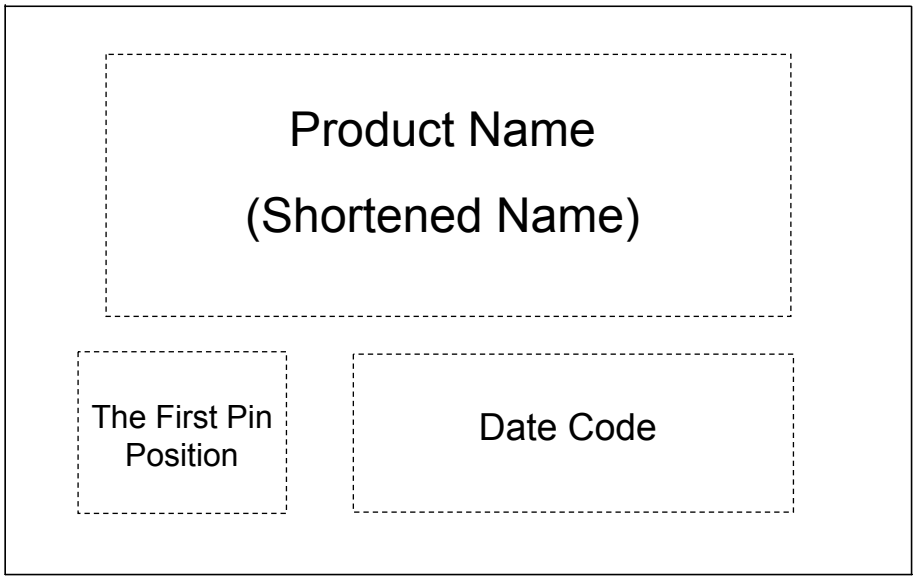



| | | |
|---|---|---|
| Body Material | : | Br / Sb Free Epoxy Resin |
| Lead Material | : | Cu Alloy |
| Lead Finish Method | : | SnBi Plating |




Established: 2006-09-01
Revised : 2009-01-29

3. Mark Drawing






Established: 2006-09-01
Revised : 2009-01-29