



# PMV48XPA2

20 V, P-channel Trench MOSFET

7 January 2020

Product data sheet

## 1. General description

P-channel enhancement mode Field-Effect Transistor (FET) in a small SOT23 (TO-236AB) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

## 2. Features and benefits

- Low threshold voltage
- Extended temperature range  $T_j = 175\text{ °C}$
- Trench MOSFET technology
- Very fast switching
- AEC-Q101 qualified

## 3. Applications

- Relay driver
- High-speed line driver
- High-side load switch
- Switching circuits

## 4. Quick reference data

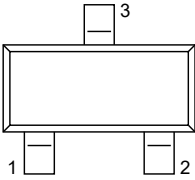
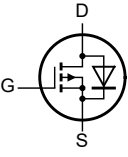
Table 1. Quick reference data

| Symbol                        | Parameter                        | Conditions                                                      | Min | Typ | Max | Unit |
|-------------------------------|----------------------------------|-----------------------------------------------------------------|-----|-----|-----|------|
| $V_{DS}$                      | drain-source voltage             | $T_j = 25\text{ °C}$                                            | -   | -   | -20 | V    |
| $V_{GS}$                      | gate-source voltage              |                                                                 | -12 | -   | 12  | V    |
| $I_D$                         | drain current                    | $V_{GS} = -4.5\text{ V}; T_{amb} = 25\text{ °C}$                | [1] | -   | -4  | A    |
| <b>Static characteristics</b> |                                  |                                                                 |     |     |     |      |
| $R_{DS(on)}$                  | drain-source on-state resistance | $V_{GS} = -4.5\text{ V}; I_D = -4\text{ A}; T_j = 25\text{ °C}$ | -   | 43  | 55  | mΩ   |

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain  $6\text{ cm}^2$ .

5. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description | Simplified outline                                                                         | Graphic symbol                                                                                   |
|-----|--------|-------------|--------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------|
| 1   | G      | gate        | <br>SOT23 | <br>017aaa257 |
| 2   | S      | source      |                                                                                            |                                                                                                  |
| 3   | D      | drain       |                                                                                            |                                                                                                  |

6. Ordering information

Table 3. Ordering information

| Type number | Package |                                                                                          |         |
|-------------|---------|------------------------------------------------------------------------------------------|---------|
|             | Name    | Description                                                                              | Version |
| PMV48XPA2   | SOT23   | plastic, surface-mounted package; 3 terminals; 1.9 mm pitch; 2.9 mm x 1.3 mm x 1 mm body | SOT23   |

7. Marking

Table 4. Marking codes

| Type number | Marking code[1] |
|-------------|-----------------|
| PMV48XPA2   | %HG             |

[1] % = placeholder for manufacturing site code

## 8. Limiting values

**Table 5. Limiting values**

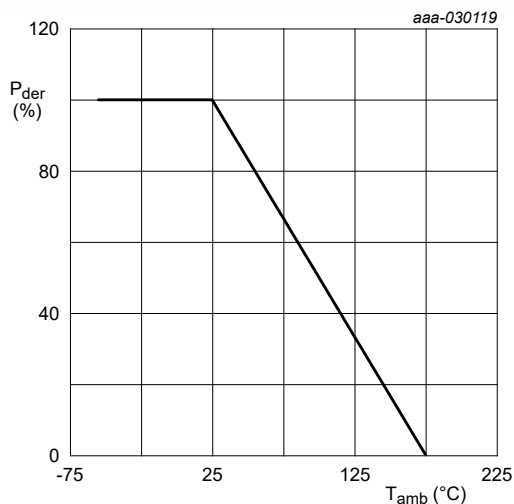
In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol                      | Parameter                                    | Conditions                                                                           |     | Min | Max  | Unit |
|-----------------------------|----------------------------------------------|--------------------------------------------------------------------------------------|-----|-----|------|------|
| V <sub>DS</sub>             | drain-source voltage                         | T <sub>j</sub> = 25 °C                                                               |     | -   | -20  | V    |
| V <sub>GS</sub>             | gate-source voltage                          |                                                                                      |     | -12 | 12   | V    |
| I <sub>D</sub>              | drain current                                | V <sub>GS</sub> = -4.5 V; T <sub>amb</sub> = 25 °C                                   | [1] | -   | -4   | A    |
|                             |                                              | V <sub>GS</sub> = -4.5 V; T <sub>amb</sub> = 100 °C                                  | [1] | -   | -2.6 | A    |
| I <sub>DM</sub>             | peak drain current                           | T <sub>amb</sub> = 25 °C; single pulse; t <sub>p</sub> ≤ 10 μs                       |     | -   | -16  | A    |
| P <sub>tot</sub>            | total power dissipation                      | T <sub>amb</sub> = 25 °C                                                             | [2] | -   | 610  | mW   |
|                             |                                              |                                                                                      | [1] | -   | 1.4  | W    |
|                             |                                              | T <sub>sp</sub> = 25 °C                                                              |     | -   | 8.3  | W    |
| T <sub>j</sub>              | junction temperature                         |                                                                                      |     | -55 | 175  | °C   |
| T <sub>amb</sub>            | ambient temperature                          |                                                                                      |     | -55 | 175  | °C   |
| T <sub>stg</sub>            | storage temperature                          |                                                                                      |     | -65 | 175  | °C   |
| <b>Source-drain diode</b>   |                                              |                                                                                      |     |     |      |      |
| I <sub>S</sub>              | source current                               | T <sub>amb</sub> = 25 °C                                                             | [1] | -   | -1.5 | A    |
| <b>ESD maximum rating</b>   |                                              |                                                                                      |     |     |      |      |
| V <sub>ESD</sub>            | electrostatic discharge voltage              | HBM                                                                                  | [3] | -   | 500  | V    |
| <b>Avalanche ruggedness</b> |                                              |                                                                                      |     |     |      |      |
| E <sub>DS(AL)S</sub>        | non-repetitive drain-source avalanche energy | T <sub>j(initial)</sub> = 25 °C; I <sub>D</sub> = -1 A; DUT in avalanche (unclamped) |     | -   | 10   | mJ   |

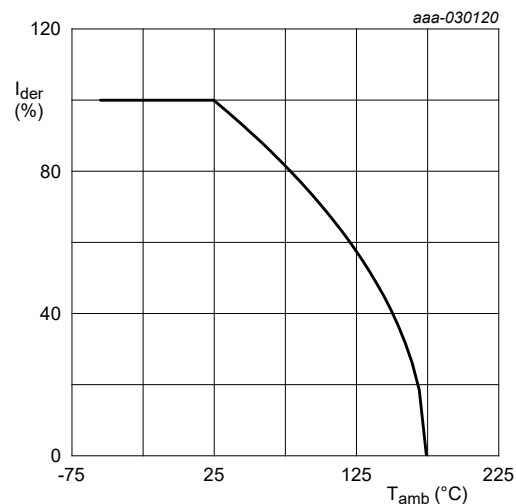
[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 6 cm<sup>2</sup>.

[2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

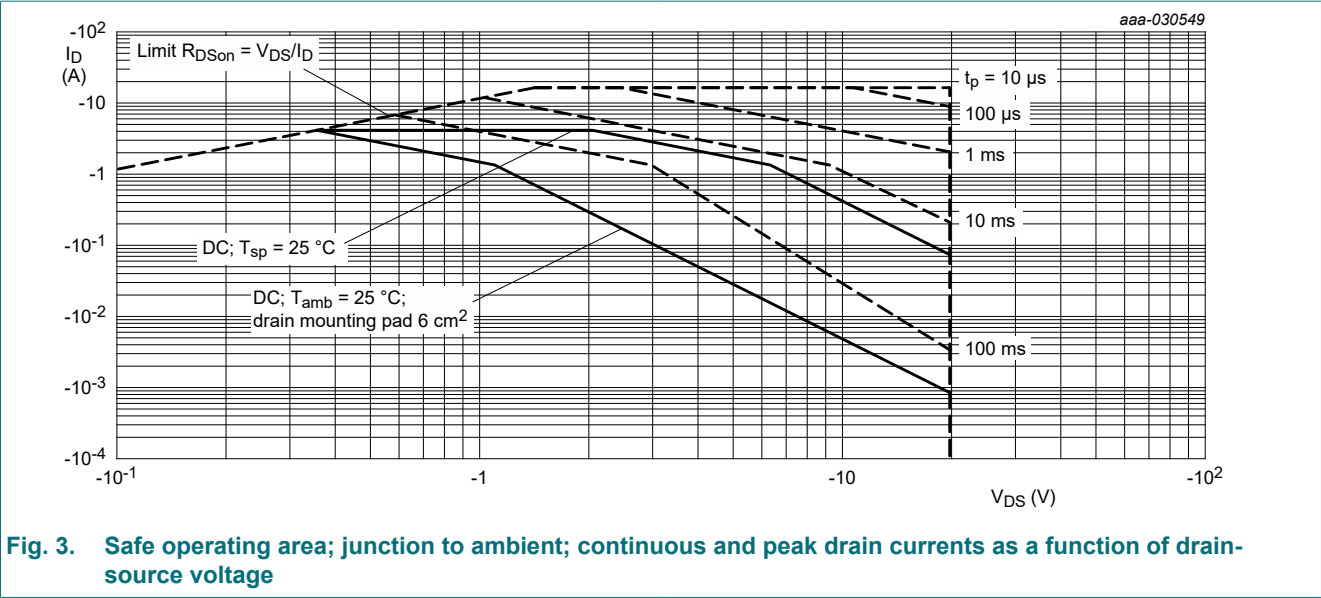
[3] Measured between all pins.



**Fig. 1. Normalized total power dissipation as a function of ambient temperature**



**Fig. 2. Normalized continuous drain current as a function of ambient temperature**



9. Thermal characteristics

Table 6. Thermal characteristics

| Symbol         | Parameter                                        | Conditions  |     | Min | Typ | Max | Unit |
|----------------|--------------------------------------------------|-------------|-----|-----|-----|-----|------|
| $R_{th(j-a)}$  | thermal resistance from junction to ambient      | in free air | [1] | -   | 208 | 245 | K/W  |
|                |                                                  |             | [2] | -   | 88  | 104 | K/W  |
| $R_{th(j-sp)}$ | thermal resistance from junction to solder point |             |     | -   | 13  | 18  | K/W  |

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.  
[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 6 cm<sup>2</sup>.

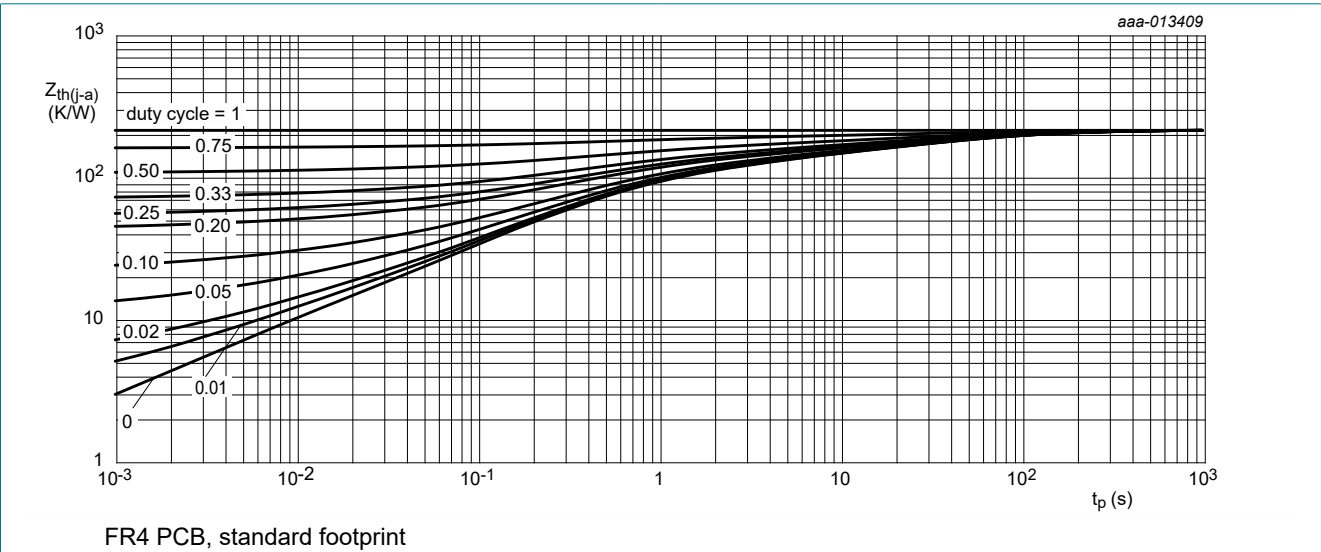


Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

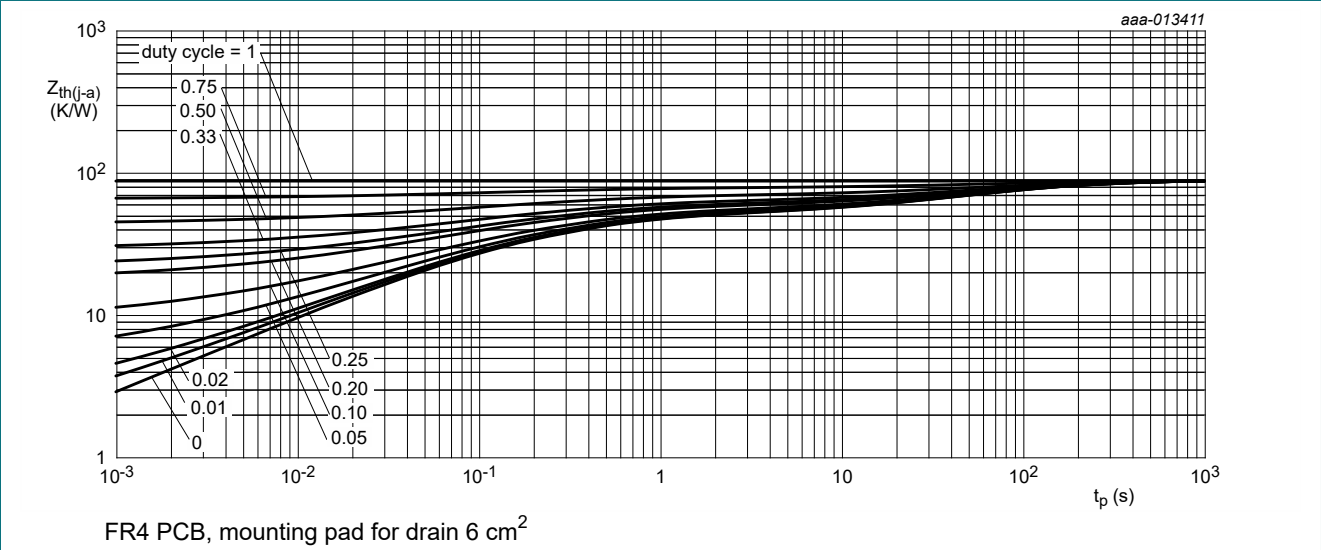


Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

## 10. Characteristics

Table 7. Characteristics

| Symbol                  | Parameter                        | Conditions                                                                                                                       |  | Min  | Typ   | Max  | Unit |
|-------------------------|----------------------------------|----------------------------------------------------------------------------------------------------------------------------------|--|------|-------|------|------|
| Static characteristics  |                                  |                                                                                                                                  |  |      |       |      |      |
| V <sub>(BR)DSS</sub>    | drain-source breakdown voltage   | I <sub>D</sub> = -250 μA; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C                                                          |  | -20  | -     | -    | V    |
| V <sub>GSth</sub>       | gate-source threshold voltage    | I <sub>D</sub> = -250 μA; V <sub>DS</sub> = V <sub>GS</sub> ; T <sub>j</sub> = 25 °C                                             |  | -0.6 | -0.95 | -1.3 | V    |
| I <sub>DSS</sub>        | drain leakage current            | V <sub>DS</sub> = -20 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C                                                           |  | -    | -     | -1   | μA   |
| I <sub>GSS</sub>        | gate leakage current             | V <sub>GS</sub> = -12 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C                                                           |  | -    | -     | -100 | nA   |
|                         |                                  | V <sub>GS</sub> = 12 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C                                                            |  | -    | -     | 100  | nA   |
| R <sub>DSon</sub>       | drain-source on-state resistance | V <sub>GS</sub> = -8 V; I <sub>D</sub> = -4 A; T <sub>j</sub> = 25 °C                                                            |  | -    | 37    | 49   | mΩ   |
|                         |                                  | V <sub>GS</sub> = -8 V; I <sub>D</sub> = -4 A; T <sub>j</sub> = 175 °C                                                           |  | -    | 59    | 78   | mΩ   |
|                         |                                  | V <sub>GS</sub> = -4.5 V; I <sub>D</sub> = -4 A; T <sub>j</sub> = 25 °C                                                          |  | -    | 43    | 55   | mΩ   |
|                         |                                  | V <sub>GS</sub> = -2.5 V; I <sub>D</sub> = -1 A                                                                                  |  | -    | 65    | 90   | mΩ   |
| g <sub>fs</sub>         | forward transconductance         | V <sub>DS</sub> = -10 V; I <sub>D</sub> = -4.2 A; T <sub>j</sub> = 25 °C                                                         |  | -    | 54    | -    | S    |
| R <sub>G</sub>          | gate resistance                  | f = 1 MHz                                                                                                                        |  | -    | 2     | -    | Ω    |
| Dynamic characteristics |                                  |                                                                                                                                  |  |      |       |      |      |
| Q <sub>G(tot)</sub>     | total gate charge                | V <sub>DS</sub> = -10 V; I <sub>D</sub> = -4.2 A; V <sub>GS</sub> = -4.5 V; T <sub>j</sub> = 25 °C                               |  | -    | 7     | 10   | nC   |
| Q <sub>GS</sub>         | gate-source charge               |                                                                                                                                  |  | -    | 1.3   | -    | nC   |
| Q <sub>GD</sub>         | gate-drain charge                |                                                                                                                                  |  | -    | 2.3   | -    | nC   |
| C <sub>iss</sub>        | input capacitance                | V <sub>DS</sub> = -10 V; f = 1 MHz; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C                                                |  | -    | 679   | -    | pF   |
| C <sub>oss</sub>        | output capacitance               |                                                                                                                                  |  | -    | 87    | -    | pF   |
| C <sub>rss</sub>        | reverse transfer capacitance     |                                                                                                                                  |  | -    | 75    | -    | pF   |
| t <sub>d(on)</sub>      | turn-on delay time               | V <sub>DS</sub> = -10 V; I <sub>D</sub> = -4.2 A; V <sub>GS</sub> = -4.5 V; R <sub>G(ext)</sub> = 6 Ω; T <sub>j</sub> = 25 °C    |  | -    | 7     | -    | ns   |
| t <sub>r</sub>          | rise time                        |                                                                                                                                  |  | -    | 19    | -    | ns   |
| t <sub>d(off)</sub>     | turn-off delay time              |                                                                                                                                  |  | -    | 26    | -    | ns   |
| t <sub>f</sub>          | fall time                        |                                                                                                                                  |  | -    | 13    | -    | ns   |
| Source-drain diode      |                                  |                                                                                                                                  |  |      |       |      |      |
| V <sub>SD</sub>         | source-drain voltage             | I <sub>S</sub> = -1.5 A; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C                                                           |  | -    | -0.8  | -1.2 | V    |
| t <sub>rr</sub>         | reverse recovery time            | I <sub>S</sub> = -1.7 A; dI <sub>S</sub> /dt = -100 A/μs; V <sub>GS</sub> = 0 V; V <sub>DS</sub> = -10 V; T <sub>j</sub> = 25 °C |  | -    | 10    | -    | ns   |
| Q <sub>r</sub>          | recovered charge                 |                                                                                                                                  |  | -    | 2     | -    | nC   |

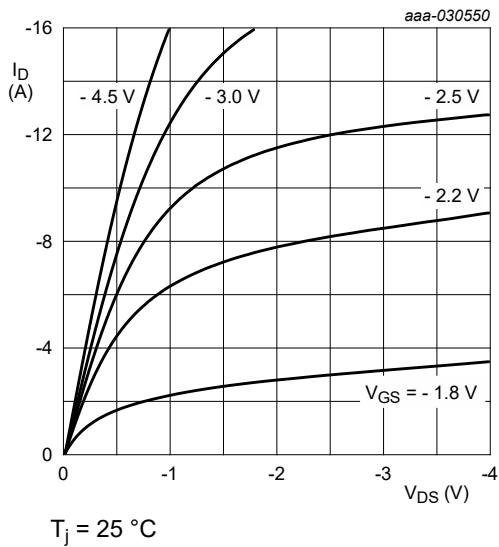


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

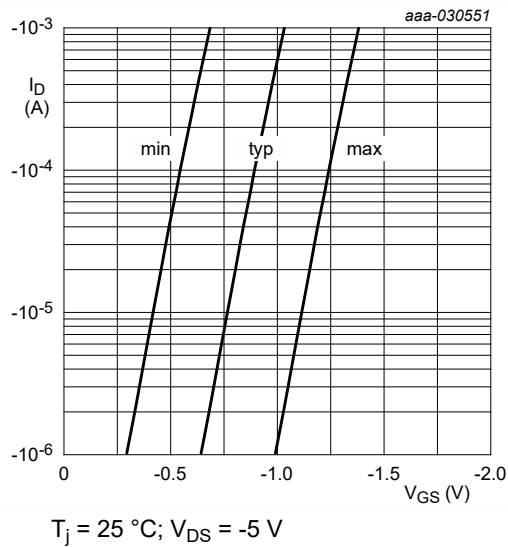


Fig. 7. Subthreshold drain current as a function of gate-source voltage

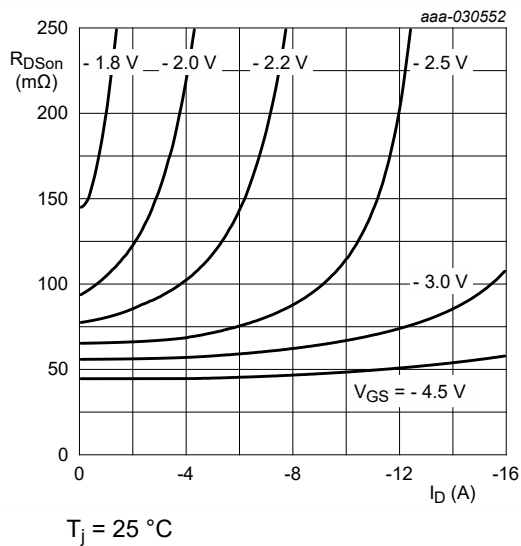


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

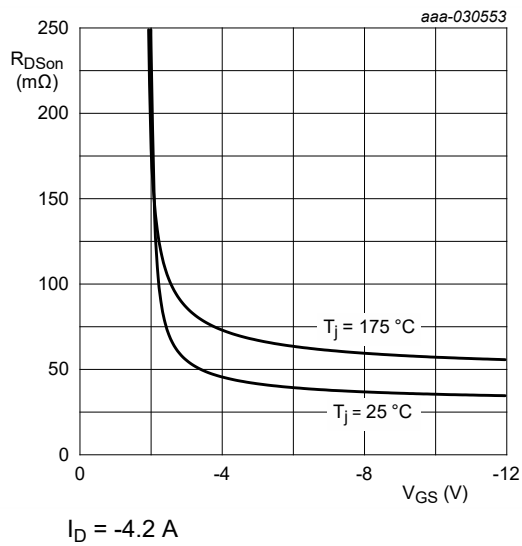


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

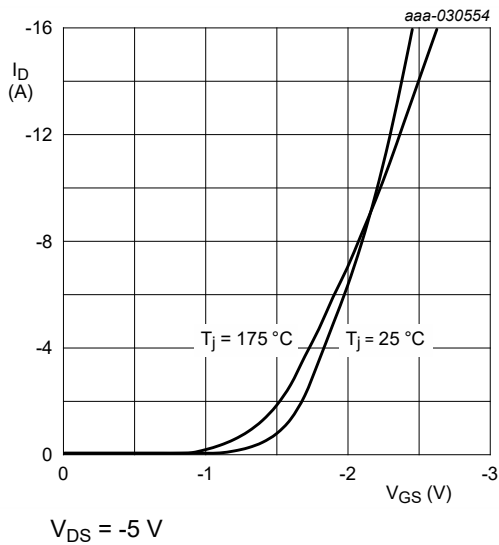


Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

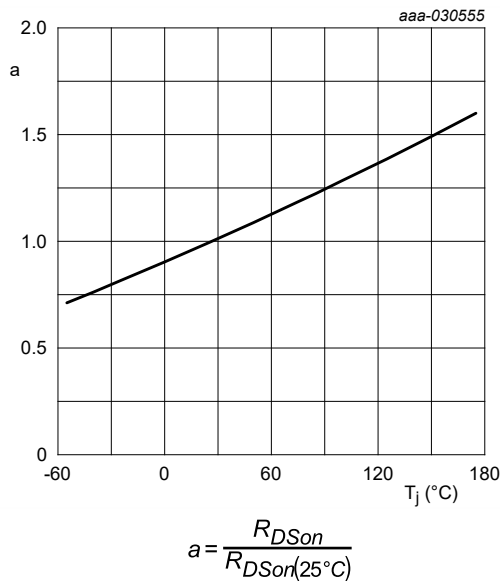


Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values

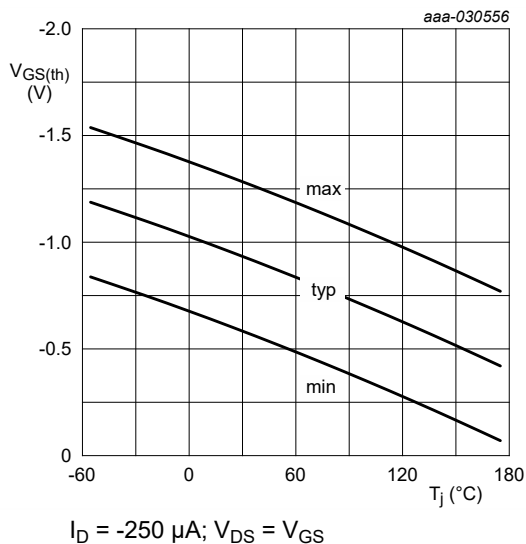


Fig. 12. Gate-source threshold voltage as a function of junction temperature

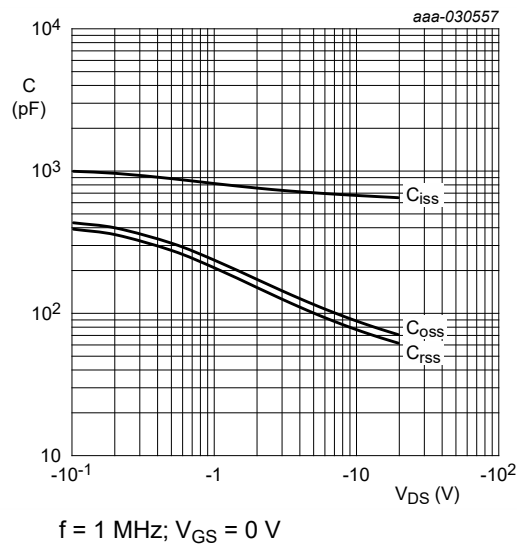


Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



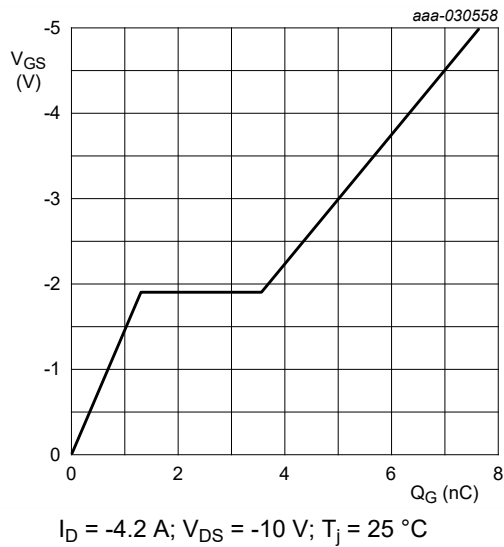


Fig. 14. Gate-source voltage as a function of gate charge; typical values

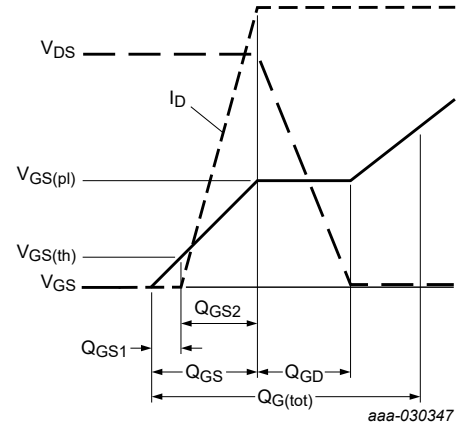


Fig. 15. Gate charge waveform definitions

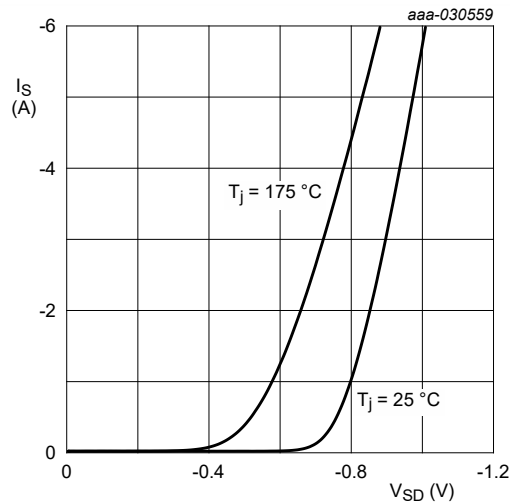


Fig. 16. Source current as a function of source-drain voltage; typical values

## 11. Test information

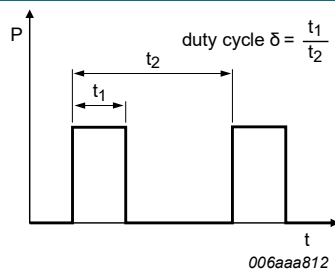


Fig. 17. Duty cycle definition

### Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q101 - Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

12. Package outline

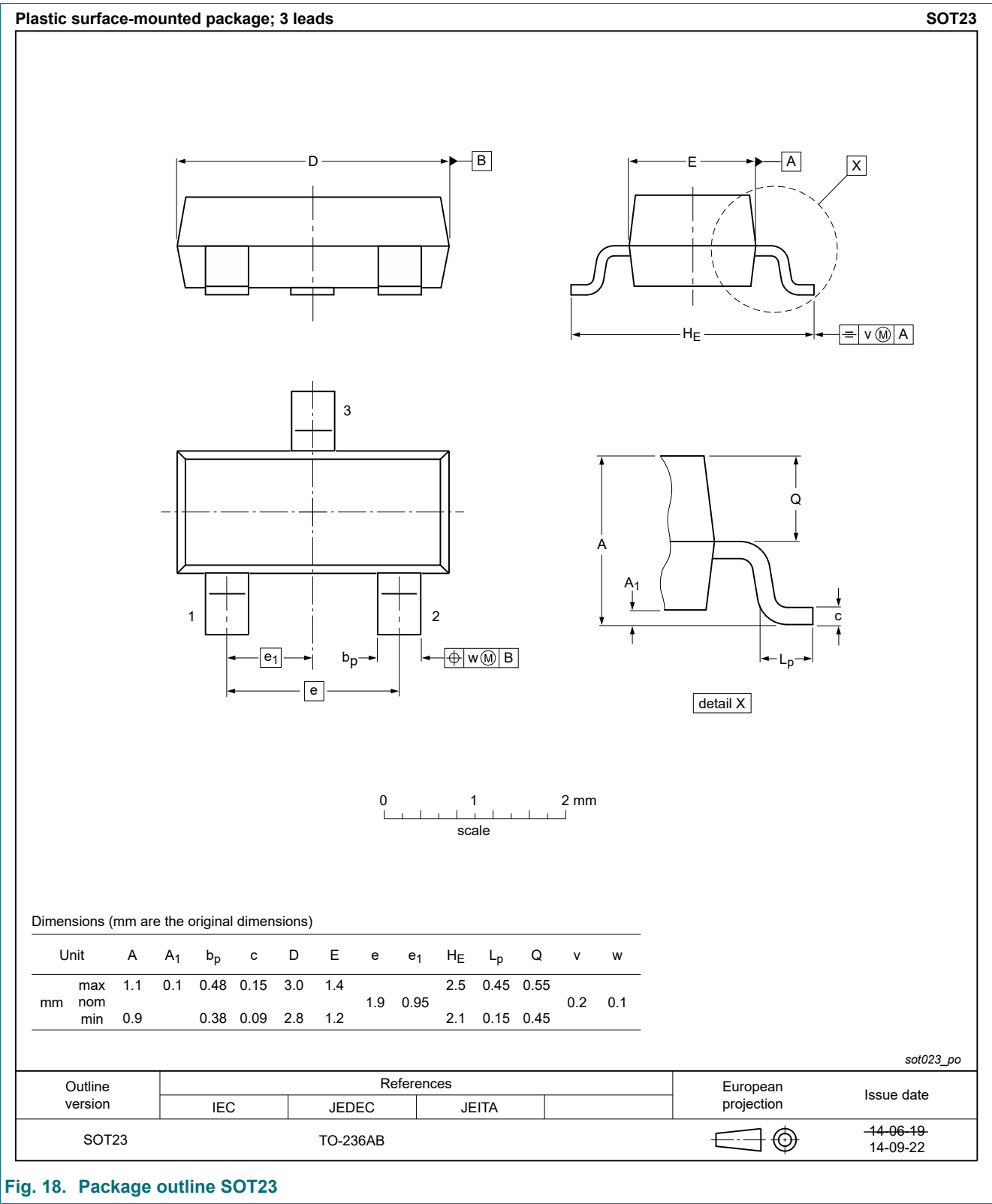


Fig. 18. Package outline SOT23

13. Soldering

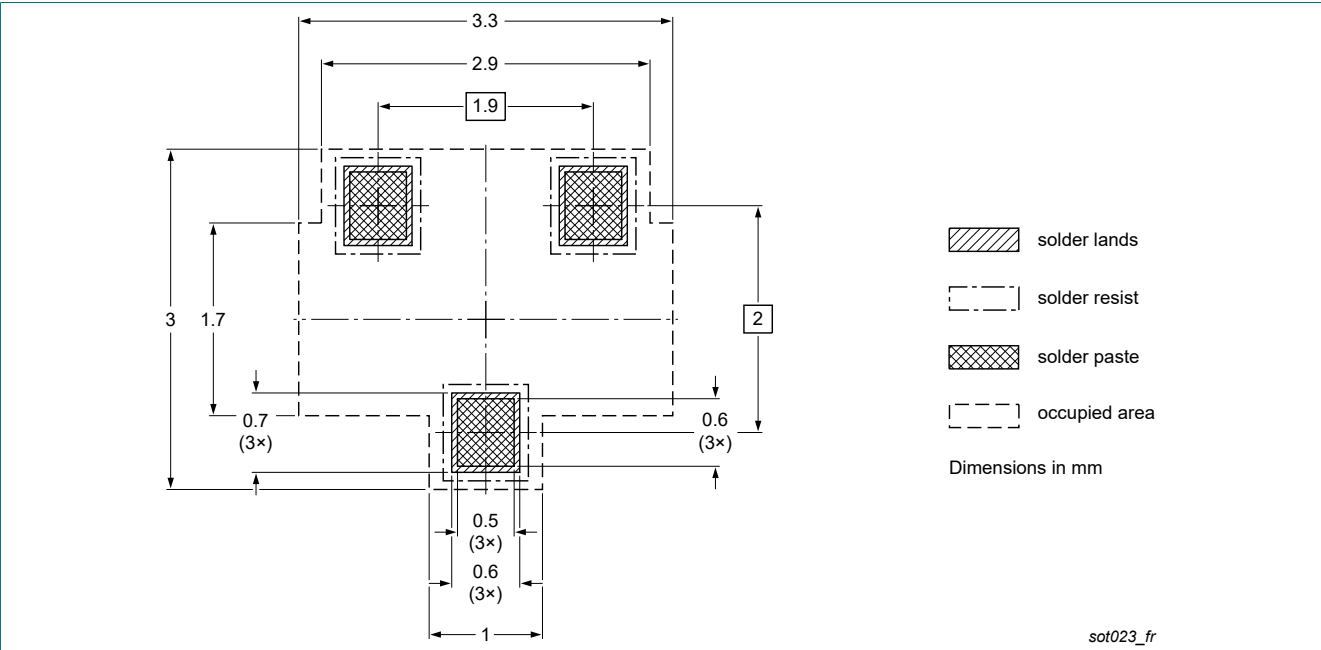


Fig. 19. Reflow soldering footprint for SOT23

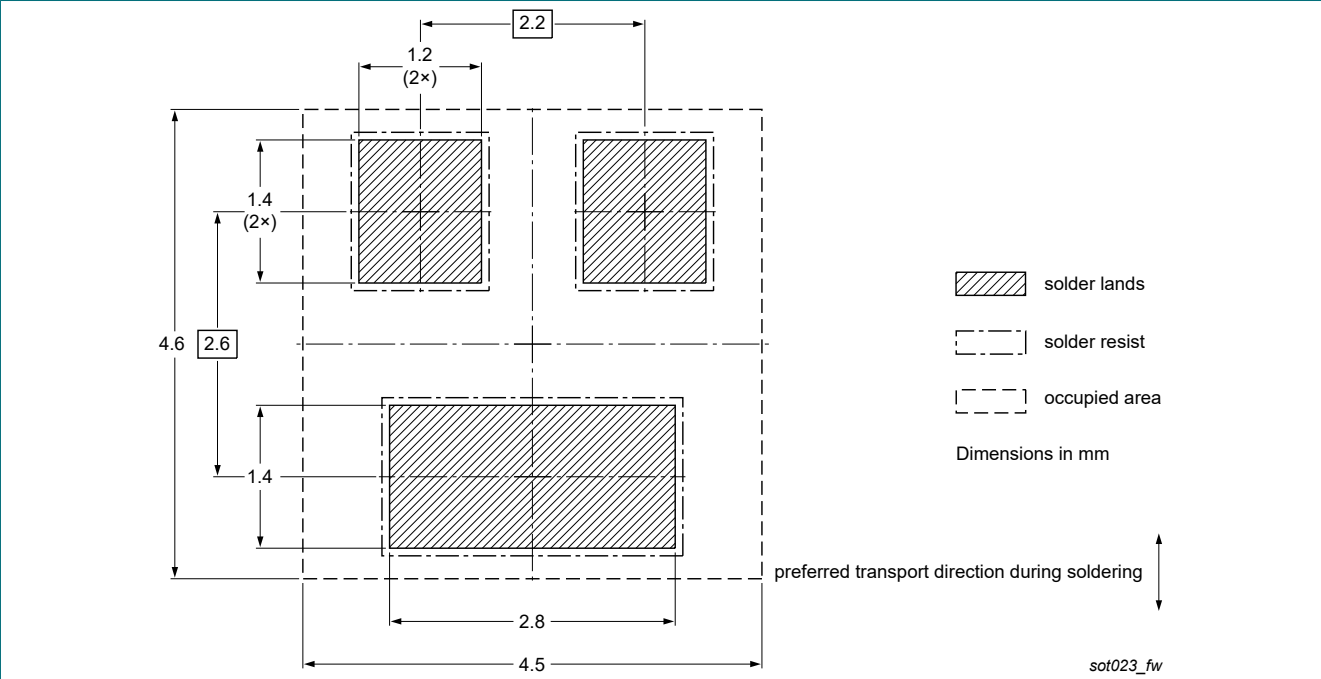


Fig. 20. Wave soldering footprint for SOT23

## 14. Revision history

Table 8. Revision history

| Data sheet ID | Release date | Data sheet status  | Change notice | Supersedes |
|---------------|--------------|--------------------|---------------|------------|
| PMV48XPA2 v.1 | 20200107     | Product data sheet | -             | -          |

## 15. Legal information

### Data sheet status

| Document status<br>[1][2]      | Product status [3] | Definition                                                                            |
|--------------------------------|--------------------|---------------------------------------------------------------------------------------|
| Objective [short] data sheet   | Development        | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification      | This document contains data from the preliminary specification.                       |
| Product [short] data sheet     | Production         | This document contains the product specification.                                     |

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