

Vishay Siliconix

Automotive N-Channel 100 V (D-S) 175 °C MOSFET

PRODUCT SUMMARY				
V _{DS} (V)	100			
$R_{DS(on)}$ (Ω) at $V_{GS} = 10 \text{ V}$	0.0110			
$R_{DS(on)}$ (Ω) at $V_{GS} = 4.5 \text{ V}$	0.0140			
I _D (A)	32			
Configuration	Single			

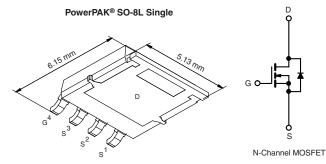
FEATURES

- TrenchFET® Power MOSFET
- AEC-Q101 Qualified^d
- 100 % R_g and UIS Tested
- Material categorization:
 For definitions of compliance please see www.vishay.com/doc?99912





ROHS COMPLIANT HALOGEN FREE



ORDERING INFORMATION	
Package	PowerPAK SO-8L
Lead (Pb)-free and Halogen-free	SQJ402EP-T1-GE3

ABSOLUTE MAXIMUM RATING	S (T _C = 25 °C, unles	s otherwise noted	d)		
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-Source Voltage		V _{DS}	100	V	
Gate-Source Voltage		V_{GS}	± 20	V	
Continuous Drain Currenta	T _C = 25 °C	1	32		
Continuous Drain Current	T _C = 125 °C	l _D	32		
Continuous Source Current (Diode Conduction) ^a		Is	32	Α	
Pulsed Drain Current ^b		I _{DM}	75		
Single Pulse Avalanche Current	1 0.1 ml l	I _{AS}	31		
Single Pulse Avalanche Energy L = 0.1 mH		E _{AS}	48	mJ	
Maximum Dawar Dissination	T _C = 25 °C	D	83	W	
Maximum Power Dissipation ^b	T _C = 125 °C	P_{D}	27	VV	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to + 175	°C	
Soldering Recommendations (Peak Temperature) ^{e, f}			260		

THERMAL RESISTANCE RATINGS				
PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-Ambient	PCB Mount ^c	R_{thJA}	65	°C/W
Junction-to-Case (Drain)		R_{thJC}	1.8	C/VV

Notes

- a. Package limited.
- b. Pulse test; pulse width $\leq 300~\mu s,~duty~cycle \leq 2~\%.$
- c. When mounted on 1" square PCB (FR-4 material).
- d. Parametric verification ongoing.
- e. See solder profile (www.vishay.com/doc?73257). The PowerPAK SO-8L is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- f. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.



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PARAMETER	SYMBOL	TES	TEST CONDITIONS		TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} :	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		-	-	V
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} =	= V _{GS} , I _D = 250 μA	1.5	2.0	2.5	V
Gate-Source Leakage	I _{GSS}	V _{DS} =	: 0 V, V _{GS} = ± 20 V	-	-	± 100	nA
		$V_{GS} = 0 V$	V _{DS} = 100 V	-	-	1	
Zero Gate Voltage Drain Current	I _{DSS}	$V_{GS} = 0 V$	V _{DS} = 100 V, T _J = 125 °C	-	-	50	μΑ
		$V_{GS} = 0 V$	V _{DS} = 100 V, T _J = 175 °C	-	-	150	
On-State Drain Current ^a	I _{D(on)}	V _{GS} = 10 V	$V_{DS} \ge 5 V$	30	-	-	Α
		V _{GS} = 10 V	I _D = 10.7 A	-	0.0090	0.0110	
Drain Cauras On State Besistance	Б	V _{GS} = 10 V	I _D = 10.7 A, T _J = 125 °C	-	-	0.0170	
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V	I _D = 10.7 A, T _J = 175 °C	-	-	0.0210	Ω
		V _{GS} = 4.5 V	I _D = 9.5 A	-	0.0115	0.0140	
Forward Transconductanceb	9 _{fs}	V _{DS} = 15 V, I _D = 10.7 A		-	54	-	S
Dynamic ^b							
Input Capacitance	C _{iss}			-	1829	2286	
Output Capacitance	C _{oss}	$V_{GS} = 0 V$	V _{DS} = 25 V, f = 1 MHz	-	722	903	pF
Reverse Transfer Capacitance	C _{rss}			-	62	78	
Total Gate Charge ^c	Qg			-	34	51	
Gate-Source Charge ^c	Q _{gs}	V _{GS} = 10 V	$V_{DS} = 50 \text{ V}, I_{D} = 10 \text{ A}$	-	6	-	nC
Gate-Drain Charge ^c	Q _{gd}]		-	13	-	
Gate Resistance	R _g		f = 1 MHz	0.65	1.39	2	Ω
Turn-On Delay Time ^c	t _{d(on)}			-	10	15	
Rise Time ^c	t _r	V_{DD}	= 50 V, $R_1 = 5 \Omega$	-	10	15	
Turn-Off Delay Time ^c	t _{d(off)}		$V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$	-	27	40	ns
Fall Time ^c	t _f	1		-	7	11	
Source-Drain Diode Ratings and Chara	octeristics ^b						
Pulsed Current ^a	I _{SM}			-	-	75	Α
Forward Voltage	V _{SD}	I _F = 7 A, V _{GS} = 0 V		_	0.77	1.2	V

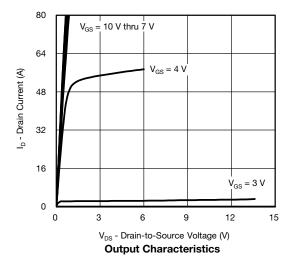
Notes

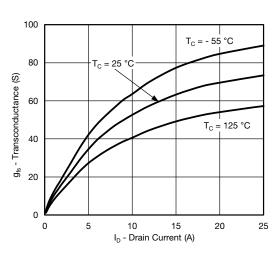
- g. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %.
- h. Guaranteed by design, not subject to production testing.
- i. Independent of operating temperature.

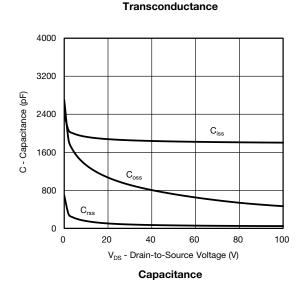
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

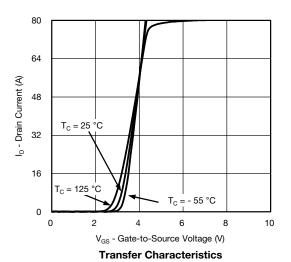


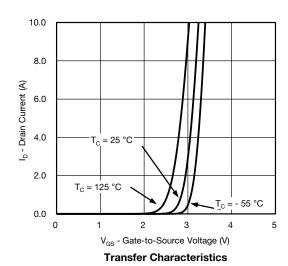
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)

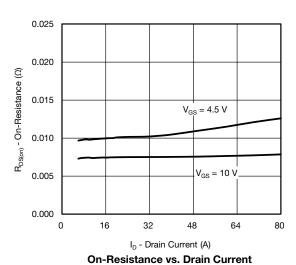






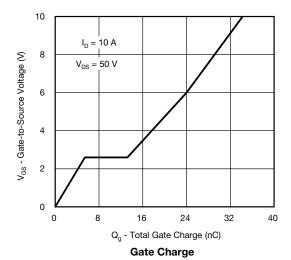


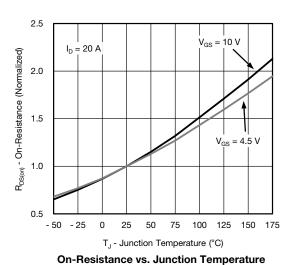


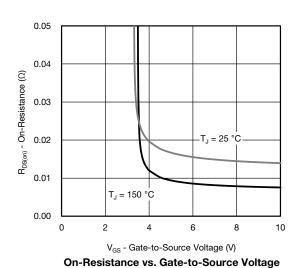


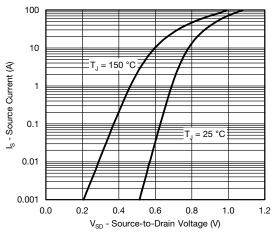


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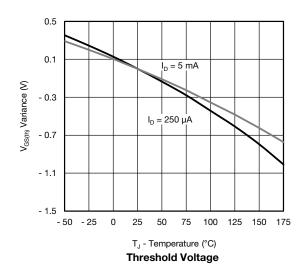


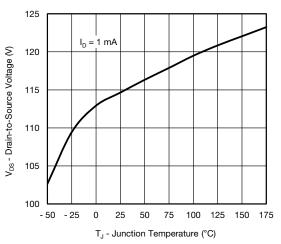








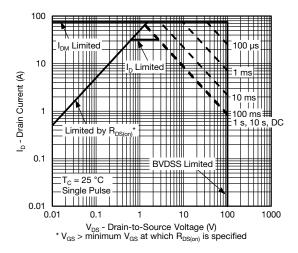




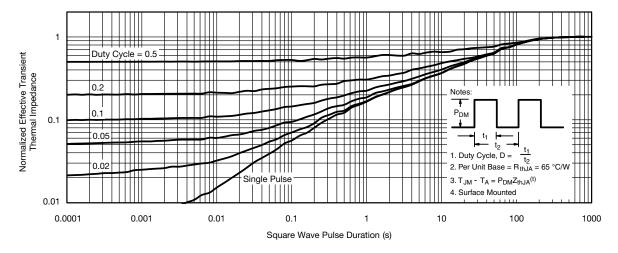
Drain Source Breakdown vs. Junction Temperature



THERMAL RATINGS ($T_A = 25$ °C, unless otherwise noted)



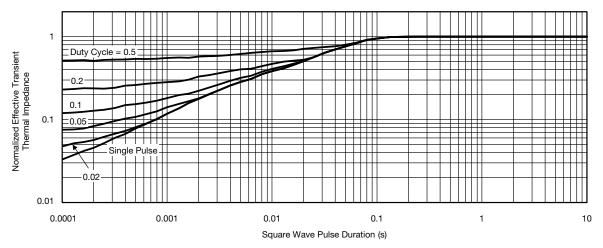
Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient

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THERMAL RATINGS (T_A = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case

Note

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
- Normalized Transient Thermal Impedance Junction-to-Case (25 °C)

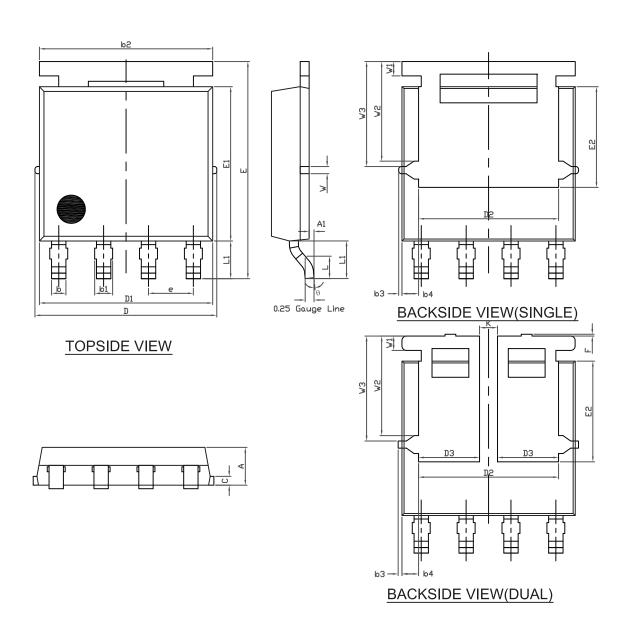
are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg267997.

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PowerPAK® SO-8L Case Outline



Package Information

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DIM.	MILLIMETERS				INCHES	
DIWI.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
А	1.00	1.07	1.14	0.039	0.042	0.045
A1	0.00	-	0.127	0.00	-	0.005
b	0.33	0.41	0.48	0.013	0.016	0.019
b1	0.44	0.51	0.58	0.017	0.020	0.023
b2	4.80	4.90	5.00	0.189	0.193	0.197
b3		0.094			0.004	
b4		0.47			0.019	
С	0.20	0.25	0.30	0.008	0.010	0.012
D	5.00	5.13	5.25	0.197	0.202	0.207
D1	4.80	4.90	5.00	0.189	0.193	0.197
D2	3.86	3.96	4.06	0.152	0.156	0.160
D3	1.63	1.73	1.83	0.064	0.068	0.072
е	1.27 BSC			0.050 BSC		
E	6.05	6.15	6.25	0.238	0.242	0.246
E1	4.27	4.37	4.47	0.168	0.172	0.176
E2 (for Al product)	2.75	2.85	2.95	0.108	0.112	0.116
E2 (for other product)	3.18	3.28	3.38	0.125	0.129	0.133
F	-	-	0.15	-	-	0.006
L	0.62	0.72	0.82	0.024	0.028	0.032
L1	0.92	1.07	1.22	0.036	0.042	0.048
K	0.51		0.020			
W	0.23		0.009			
W1	0.41		0.016			
W2	2.82		0.111			
W3		2.96		0.117		
θ	0°	-	10°	0°	-	10°

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DWG: 5976

Note

• Millimeters will gover



RECOMMENDED MINIMUM PAD FOR PowerPAK® SO-8L SINGLE



Recommended Minimum Pads Dimensions in mm (inches)



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Please note that some Vishay documentation may still make reference to RoHS Directive 2002/95/EC. We confirm that all the products identified as being compliant to Directive 2002/95/EC conform to Directive 2011/65/EU.

Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as Halogen-Free follow Halogen-Free requirements as per JEDEC JS709A standards. Please note that some Vishay documentation may still make reference to the IEC 61249-2-21 definition. We confirm that all the products identified as being compliant to IEC 61249-2-21 conform to JEDEC JS709A standards.

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