STM32F042xx

ARM-based 32-bit MCU, up to 32 KB Flash, crystal-less USB FS 2.0, CAN, 8 timers, ADC & comm. interfaces, 2.0 - 3.6 V

Data brief - preliminary data

Features

- Core: ARM® 32-bit Cortex™-M0 CPU, frequency up to 48 MHz
- Memories
  - 16 to 32 Kbytes of Flash memory
  - 6 Kbytes of SRAM with HW parity checking
- CRC calculation unit
- Reset and power management
  - Voltage range: 2.0 V to 3.6 V
  - Power-on/Power down reset (POR/PDR)
  - Programmable voltage detector (PVD)
  - Low power modes: Sleep, Stop, Standby
  - V_{BAT} supply for RTC and backup registers
- Clock management
  - 4 to 32 MHz crystal oscillator
  - 32 kHz oscillator for RTC with calibration
  - Internal 8 MHz RC with x6 PLL option
  - Internal 40 kHz RC oscillator
  - Internal 48 MHz oscillator with automatic trimming based on ext. synchronization
- Up to 37 fast I/Os
  - All mappable on external interrupt vectors
  - Up to 37 I/Os with 5-V tolerant capability and 8 with independent supply V_{DDIO2}
- 5-channel DMA controller
- One 12-bit, 1.0 µs ADC (up to 10 channels)
  - Conversion range: 0 to 3.6 V
  - Separate analog supply from 2.4 up to 3.6
- Up to 15 capacitive sensing channels for touchkey, linear and rotary touch sensors
- Calendar RTC with alarm and periodic wakeup from Stop/Standby
- 8 timers
  - One 16-bit advanced-control timer for 6 channel PWM output

LQFP48 7x7
LQFP32 5x5

UFQFPN48 7x7
UFQFPN32 5x5
UFQFPN28 4x4

WLCSP36

TSSOP20

  - One 32-bit and four 16-bit timers, with up to 4 IC/OC, OCN, usable for IR control decoding
  - Independent and system watchdog timers
  - SysTick timer
- Communication interfaces
  - One I^2C interface supporting Fast Mode Plus (1 Mbit/s) with 20 mA current sink, SMBus/PMBus and wakeup
  - Two USARTs supporting master synchronous SPI and modem control; one with ISO7816 interface, LIN, IrDA, auto baud rate detection and wakeup feature
  - Two SPIs (18 Mbit/s) with 4 to 16 programmable bit frames, and with I^2S interface multiplexed
  - CAN interface
  - USB 2.0 full-speed interface, able to run from internal 48 MHz oscillator and with BCD and LPM support
- HDMI CEC, wakeup on header reception
- Serial wire debug (SWD)
- 96-bit unique ID
- All packages ECOPACK®2

Table 1. Device summary

Reference	Part number
STM32F042xx	STM32F042F4, STM32F042G4, STM32F042K4, STM32F042T4, STM32F042C4 STM32F042F6, STM32F042G6, STM32F042K6, STM32F042T6, STM32F042C6

Contents

1 Introduction 6

2 Description 7

3 Functional overview 10

3.1 ARM® CortexTM-M0 core with embedded Flash and SRAM 10

3.2 Memories 10

3.3 Boot modes 10

3.4 Cyclic redundancy check calculation unit (CRC) 11

3.5 Power management 11

3.5.1 Power supply schemes 11

3.5.2 Power supply supervisors 11

3.5.3 Voltage regulator 12

3.5.4 Low-power modes 12

3.6 Clocks and startup 13

3.7 General-purpose inputs/outputs (GPIOs) 14

3.8 Direct memory access controller (DMA) 15

3.9 Interrupts and events 15

3.9.1 Nested vectored interrupt controller (NVIC) 15

3.9.2 Extended interrupt/event controller (EXTI) 15

3.10 Analog to digital converter (ADC) 15

3.10.1 Temperature sensor 16

3.10.2 Internal voltage reference (V_{REFINT}) 16

3.10.3 V_{BAT} battery voltage monitoring 16

3.11 Touch sensing controller (TSC) 17

3.12 Timers and watchdogs 18

3.12.1 Advanced-control timer (TIM1) 19

3.12.2 General-purpose timers (TIM2..3, TIM14, 16, 17) 19

3.12.3 Independent watchdog (IWDG) 20

3.12.4 System window watchdog (WWDG) 20

3.12.5 SysTick timer 20

3.13 Real-time clock (RTC) and backup registers 20

3.14 Inter-integrated circuit interfaces (I^2C) 21

3.15 Universal synchronous/asynchronous receiver transmitters (USART) . . 22
3.16 Serial peripheral interface (SPI)/Inter-integrated sound interfaces (I^2S) . 23
3.17 High-definition multimedia interface (HDMI) - consumer electronics control (CEC) 24
3.18 Controller area network (CAN) 24
3.19 Universal serial bus (USB) 24
3.20 Clock recovery system (CRS) 24
3.21 Serial wire debug port (SW-DP) 24

4 Pinouts and pin descriptions 25

5 Memory mapping 38

6 Package characteristics 41
6.1 Package mechanical data 41

7 Part numbering 55

8 Revision history 56

List of tables

Table 1. Device summary . . . 1
Table 2. STM32F042xx device features and peripheral counts . . . 8
Table 3. Temperature sensor calibration values . . . 16
Table 4. Internal voltage reference calibration values . . . 16
Table 5. Capacitive sensing GPIOs available on STM32F042xx devices . . . 17
Table 6. No. of capacitive sensing channels available on STM32F042xx devices . . . 18
Table 7. Timer feature comparison . . . 18
Table 8. Comparison of I2C analog and digital filters . . . 21
Table 9. STM32F042xx I^2C implementation . . . 22
Table 10. STM32F042xx USART implementation . . . 22
Table 11. STM32F042xx SPI/I2S implementation . . . 23
Table 12. Legend/abbreviations used in the pinout table . . . 29
Table 13. STM32F042xx pin definitions . . . 29
Table 14. Alternate functions selected through GPIOA_AFR registers for port A . . . 35
Table 15. Alternate functions selected through GPIOB_AFR registers for port B . . . 36
Table 16. Alternate functions selected through GPIOF_AFR registers for port F . . . 37
Table 17. STM32F042xx peripheral register boundary addresses . . . 39
Table 18. LQFP48 – 7 x 7 mm low-profile quad flat package mechanical data . . . 41
Table 19. UFQFPN48 – 7 x 7 mm, 0.5 mm pitch, package mechanical data . . . 44
Table 20. WLCSP36, 0.4 mm pitch, package mechanical data . . . 46
Table 21. LQFP32 – 7 x 7mm 32-pin low-profile quad flat package mechanical data . . . 47
Table 22. UFQFPN32 – 5 x 5 mm, 32-lead ultra thin fine pitch quad flat no-lead package mechanical data . . . 49
Table 23. UFQFPN28 – 4 x 4 mm, 28-lead ultra thin fine pitch quad flat no-lead package mechanical data . . . 51
Table 24. TSSOP20 – 20-pin thin shrink small outline package mechanical data . . . 53
Table 25. Ordering information scheme . . . 55
Table 26. Document revision history . . . 56

List of figures

Figure 1. Block diagram . . . 9
Figure 2. Clock tree . . . 14
Figure 3. LQFP48 48-pin package pinout (top view) . . . 25
Figure 4. UFQFPN48 48-pin package pinout (top view) . . . 25
Figure 5. WLCSP36 36-pin package ball-out . . . 26
Figure 6. LQFP32 32-pin package pinout (top view) . . . 26
Figure 7. UFQFPN32 32-pin package pinout (top view) . . . 27
Figure 8. UQFPN28 28-pin package (top view) . . . 27
Figure 9. TSSOP20 20-pin package (top view) . . . 28
Figure 10. STM32F042xx memory map . . . 38
Figure 11. LQFP48 – 7 x 7 mm, 48 pin low-profile quad flat package outline . . . 41
Figure 12. LQFP48 recommended footprint . . . 42
Figure 13. UFQFPN48 – 7 x 7 mm, 0.5 mm pitch, package outline . . . 43
Figure 14. UFQFPN48 recommended footprint . . . 44
Figure 15. WLCSP36 - 0.4 mm pitch, package outline . . . 45
Figure 16. LQFP32 – 7 x 7mm 32-pin low-profile quad flat package outline . . . 47
Figure 17. LQFP32 recommended footprint . . . 48
Figure 18. UFQFPN32 - 5 x 5 mm, 32-lead ultra thin fine pitch quad flat no-lead package outline . . . 49
Figure 19. UFQFPN32 recommended footprint . . . 50
Figure 20. UFQFPN28 - 4 x 4 mm, 28-lead ultra thin fine pitch quad flat no-lead package outline . . . 51
Figure 21. UFQFPN28 recommended footprint . . . 52
Figure 22. TSSOP20 - 20-pin thin shrink small outline . . . 53
Figure 23. TSSOP20 recommended footprint . . . 54

1 Introduction

This databrief provides the ordering information and mechanical device characteristics of the STM32F042xx microcontrollers.

This document should be read in conjunction with the STM32F0xxxx reference manual (RM0091). The reference manual is available from the STMicroelectronics website www.st.com.

For information on the ARM Cortex™-M0 core, please refer to the Cortex™-M0 Technical Reference Manual, available from the www.arm.com website at the following address: http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.ddi0432c/index.html.

2 Description

The STM32F042xx microcontrollers incorporate the high-performance ARM Cortex™-M0 32-bit RISC core operating at a 48 MHz frequency, high-speed embedded memories (up to 32 Kbytes of Flash memory and 6 Kbytes of SRAM), and an extensive range of enhanced peripherals and I/Os. All devices offer standard communication interfaces (one I^2C, two SPIs/I2S, one HDMI CEC and two USARTs), one USB Full speed device (crystal-less), one CAN, one 12-bit ADC, four general-purpose 16-bit timers, a 32-bit timer and an advanced-control PWM timer.

The STM32F042xx microcontrollers operate in the -40 to +85 °C and -40 to +105 °C temperature ranges from a 2.0 to 3.6 V power supply. A comprehensive set of power-saving modes allows the design of low-power applications.

The STM32F042xx microcontrollers include devices in seven different packages ranging from 20 pins to 48 pins. Depending on the device chosen, different sets of peripherals are included. The description below provides an overview of the complete range of STM32F042xx peripherals proposed.

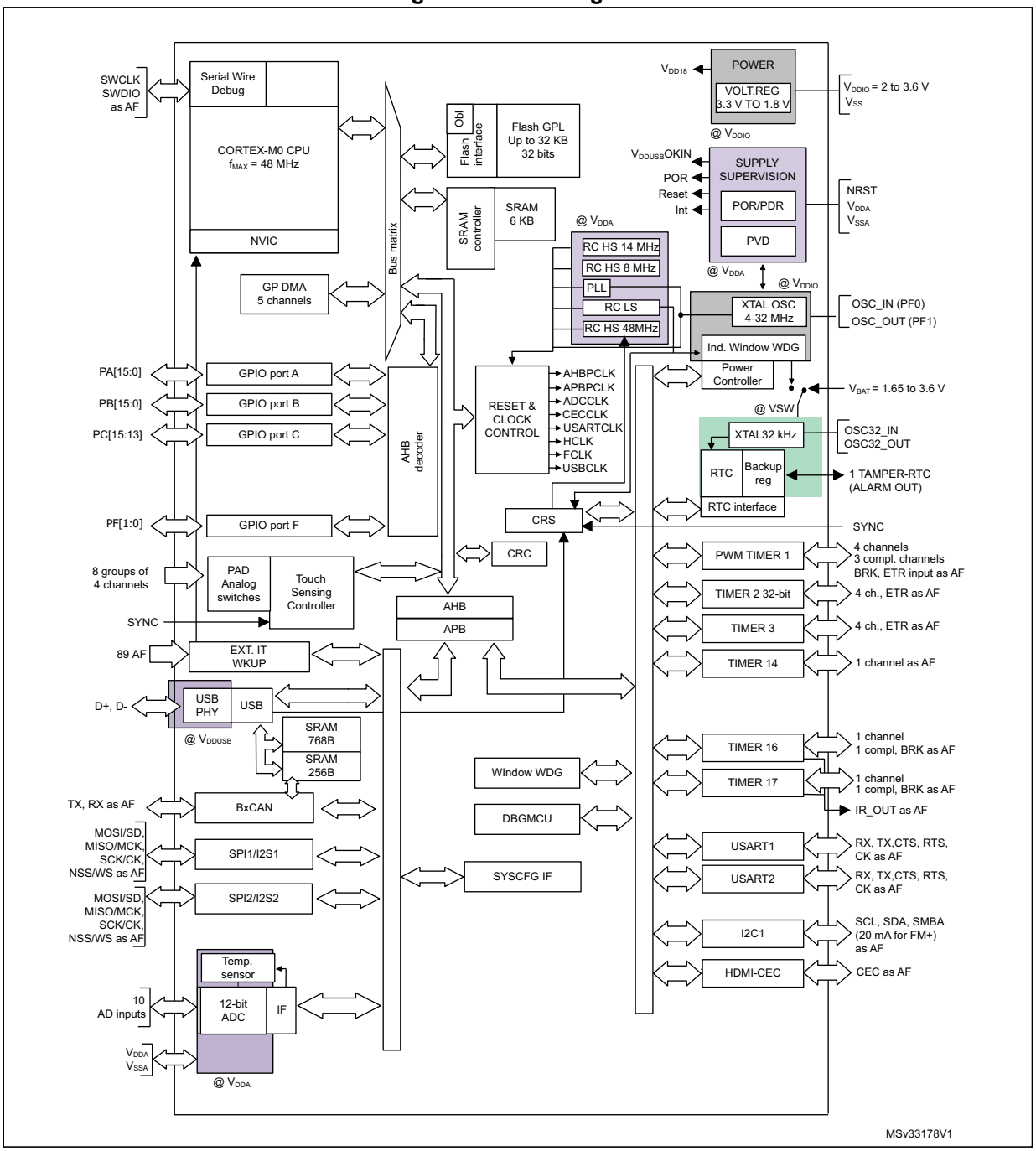
These features make the STM32F042xx microcontrollers suitable for a wide range of applications such as application control and user interfaces, handheld equipment, A/V receivers and digital TV, PC peripherals, gaming and GPS platforms, industrial applications, PLCs, inverters, printers, scanners, alarm systems, video intercoms, and HVACs.

Table 2. STM32F042xx device features and peripheral counts

Peripheral		STM32F042Fx		STM32F042G		STM32F042K		STM32F042T		STM32F042C	
Flash (Kbytes)		16	32	16	32	16	32	16	32	16	32
SRAM (Kbytes)		6		6		6		6		6	
Timers	Advanced control	1 (16-bit)									
	General purpose	4 (16-bit) 1 (32-bit)									
Comm. interfaces	SPI [I2S](1)	2[2]									
	I^2C	1									
	USART	2									
	CAN	1									
	USB	1									
	CEC	1									
12-bit ADC (number of channels)		1 (9 ext. + 3 int.)		1 (10 ext. + 3 int.)							
GPIOs		16		24		26 28		30		38	
Capacitive sensing channels		7		11		13 14		14		14	
Max. CPU frequency		48 MHz									
Operating voltage		2.0 to 3.6 V									
Operating temperature		Ambient operating temperature: -40 °C to 85 °C / -40 °C to 105 °C Junction temperature: -40 °C to 105 °C / -40 °C to 125 °C									
Packages		TSSOP20		UQFPN28		LQFP32 UQFPN32		WLCSP36		LQFP48 UFQFPN48	

1. The SPI interfaces can be used either in SPI mode or in I2S audio mode.

Figure 1. Block diagram



3 Functional overview

3.1 ARM® Cortex™-M0 core with embedded Flash and SRAM

The ARM Cortex™-M0 processor is the latest generation of ARM processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM Cortex™-M0 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The STM32F0xx family has an embedded ARM core and is therefore compatible with all ARM tools and software.

Figure 1 shows the general block diagram of the device family.

3.2 Memories

The device has the following features:

- 6 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states and featuring embedded parity checking with exception generation for fail-critical applications.
- The non-volatile memory is divided into two arrays:
  - 16 to 32 Kbytes of embedded Flash memory for programs and data
  - Option bytes

  The option bytes are used to write-protect the memory (with 4 KB granularity) and/or readout-protect the whole memory with the following options:
  - Level 0: no readout protection
  - Level 1: memory readout protection, the Flash memory cannot be read from or written to if either debug features are connected or boot in RAM is selected
  - Level 2: chip readout protection, debug features (Cortex-M0 serial wire) and boot in RAM selection disabled

3.3 Boot modes

At startup, the boot pin and boot selector option bit are used to select one of three boot options:

- Boot from User Flash
- Boot from System Memory
- Boot from embedded SRAM

The boot loader is located in System Memory. It is used to reprogram the Flash memory by using USART on pins PA14/PA15 or PA9/PA10, I2C on pins PB6/PB7 or through the USB DFU interface.

3.4 Cyclic redundancy check calculation unit (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a CRC-32 (Ethernet) polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

3.5 Power management

3.5.1 Power supply schemes

- V_{DD} = 2.0 to 3.6 V: external power supply for I/Os. Provided externally through V_{DD} pins.
- V_{DDA} = 2.0 to 3.6 V: external analog power supply for ADC, Reset blocks, RCs and PLL (minimum voltage to be applied to V_{DDA} is 2.4 V when the ADC and DAC are used). The V_{DDA} voltage level must be always greater or equal to the V_{DD} voltage level and must be provided first.
- V_{DDIO2} = 1.65 to 3.6 V: external power supply for marked I/Os. Provided externally through the VDDIO2 pin. The V_{DDIO2} voltage level is completely independent from V_{DD} or V_{DDA}, but it must not be provided without a valid supply on V_{DD}. Refer to the pinout diagrams or tables for concerned I/Os list.
- V_{BAT} = 1.65 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

3.5.2 Power supply supervisors

The device has integrated power-on reset (POR) and power-down reset (PDR) circuits. They are always active, and ensure proper operation above a threshold of 2 V. The device remains in reset mode when the monitored supply voltage is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit.

- The POR monitors only the V_{DD} supply voltage. During the startup phase it is required that V_{DDA} should arrive first and be greater than or equal to V_{DD}.
- The PDR monitors both the V_{DD} and V_{DDA} supply voltages, however the V_{DDA} power supply supervisor can be disabled (by programming a dedicated Option bit) to reduce the power consumption if the application design ensures that V_{DDA} is higher than or equal to V_{DD}.

The V_{DDIO2} supply is monitored and compared with the internal reference voltage (V_{REFINT}). When the V_{DDIO2} is below this threshold, all the I/Os supplied from this rail are disabled by hardware. The output of this comparator is connected to EXTI line 31 and it can be used to generate an interrupt.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD} drops below the V_{PVD} threshold and/or when V_{DD} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.5.3 Voltage regulator

The regulator has two operating modes and it is always enabled after reset.

- Main (MR) is used in normal operating mode (Run).
- Low power (LPR) can be used in Stop mode where the power demand is reduced.

In Standby mode, it is put in power down mode. In this mode, the regulator output is in high impedance and the kernel circuitry is powered down, inducing zero consumption (but the contents of the registers and SRAM are lost).

3.5.4 Low-power modes

The STM32F042xx microcontrollers support three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep mode**

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Stop mode**

  Stop mode achieves very low power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low power mode.

  The device can be woken up from Stop mode by any of the EXTI lines. The EXTI line source can be one of the 16 external lines, the PVD output, RTC alarm, COMPx, I2C1, USART1 or the CEC.

  The I2C1, USART1 and the CEC can be configured to enable the HSI RC oscillator for processing incoming data. If this is used when the voltage regulator is put in low power mode, the regulator is first switched to normal mode before the clock is provided to the given peripheral.

- **Standby mode**

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the RTC domain and Standby circuitry.

  The device exits Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pins, or an RTC event occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.

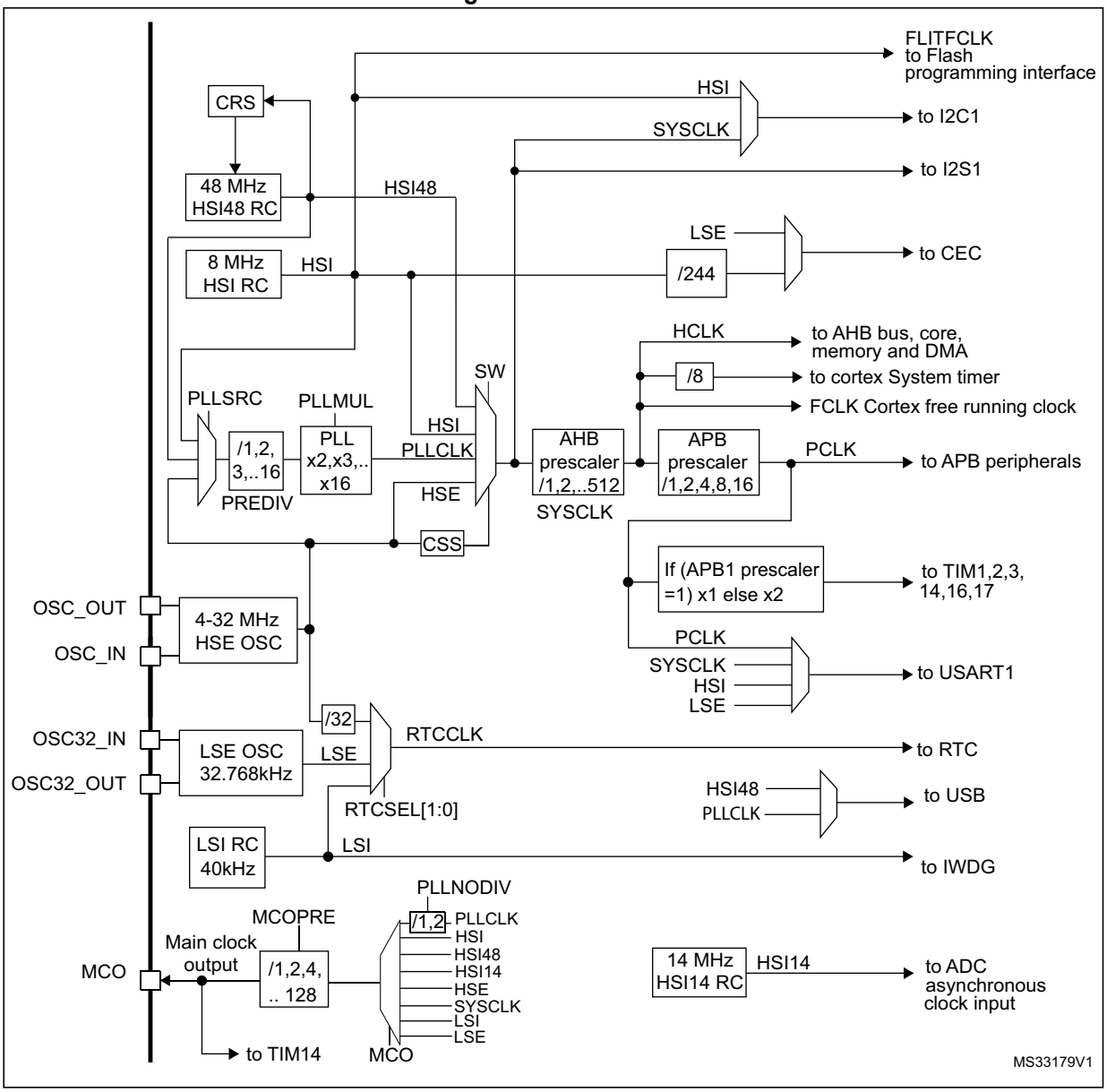
3.6 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-32 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example on failure of an indirectly used external crystal, resonator or oscillator).

Several prescalers allow the application to configure the frequency of the AHB and the APB domains. The maximum frequency of the AHB and the APB domains is 48 MHz.

Additionally, also the internal RC 48 MHz oscillator can be selected for system clock or PLL input source. This oscillator can be automatically fine-trimmed by the means of the CRS peripheral using the external synchronization.

Figure 2. Clock tree



3.7 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions.

The I/O configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

3.8 Direct memory access controller (DMA)

The 5-channel general-purpose DMAs manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers.

The DMA supports circular buffer management, removing the need for user code intervention when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

DMA can be used with the main peripherals: SPI, I2S, I2C, USART, all TIMx timers (except TIM14) and ADC.

3.9 Interrupts and events

3.9.1 Nested vectored interrupt controller (NVIC)

The STM32F0xx family embeds a nested vectored interrupt controller able to handle up to 32 maskable interrupt channels (not including the 16 interrupt lines of Cortex™-M0) and 4 priority levels.

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

3.9.2 Extended interrupt/event controller (EXTI)

The extended interrupt/event controller consists of 24 edge detector lines used to generate interrupt/event requests and wake-up the system. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the internal clock period. Up to 38 GPIOs can be connected to the 16 external interrupt lines.

3.10 Analog to digital converter (ADC)

The 12-bit analog to digital converter has up to 10 external and 3 internal (temperature sensor, voltage reference, VBAT voltage measurement) channels and performs conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

3.10.1 Temperature sensor

The temperature sensor (TS) generates a voltage V_{SENSE} that varies linearly with temperature.

The temperature sensor is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode.

Table 3. Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at a temperature of 30 °C (± 5 °C), V_{DDA}= 3.3 V (± 10 mV)	0x1FFF F7B8 - 0x1FFF F7B9
TS_CAL2	TS ADC raw data acquired at a temperature of 110 °C (± 5 °C), V_{DDA}= 3.3 V (± 10 mV)	0x1FFF F7C2 - 0x1FFF F7C3

3.10.2 Internal voltage reference (V_{REFINT})

The internal voltage reference (V_{REFINT}) provides a stable (bandgap) voltage output for the ADC and Comparators. V_{REFINT} is internally connected to the ADC_IN17 input channel. The precise voltage of V_{REFINT} is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode.

Table 4. Internal voltage reference calibration values

Calibration value name	Description	Memory address
VREFINT_CAL	Raw data acquired at a temperature of 30 °C (± 5 °C), V_{DDA}= 3.3 V (± 10 mV)	0x1FFF F7BA - 0x1FFF F7BB

3.10.3 V_{BAT} battery voltage monitoring

This embedded hardware feature allows the application to measure the V_{BAT} battery voltage using the internal ADC channel ADC_IN18. As the V_{BAT} voltage may be higher than V_{DDA}, and thus outside the ADC input range, the V_{BAT} pin is internally connected to a bridge divider by 2. As a consequence, the converted digital value is half the V_{BAT} voltage.

3.11 Touch sensing controller (TSC)

The STM32F042xx devices provide a simple solution for adding capacitive sensing functionality to any application. These devices offer up to 14 capacitive sensing channels distributed over 5 analog I/O groups.

Capacitive sensing technology is able to detect the presence of a finger near a sensor which is protected from direct touch by a dielectric (glass, plastic...). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle. It consists of charging the sensor capacitance and then transferring a part of the accumulated charges into a sampling capacitor until the voltage across this capacitor has reached a specific threshold. To limit the CPU bandwidth usage, this acquisition is directly managed by the hardware touch sensing controller and only requires few external components to operate.

The touch sensing controller is fully supported by the STMTouch touch sensing firmware library, which is free to use and allows touch sensing functionality to be implemented reliably in the end application.

Table 5. Capacitive sensing GPIOs available on STM32F042xx devices

Group	Capacitive sensing signal name	Pin name
1	TSC_G1_IO1	PA0
	TSC_G1_IO2	PA1
	TSC_G1_IO3	PA2
	TSC_G1_IO4	PA3
2	TSC_G2_IO1	PA4
	TSC_G2_IO2	PA5
	TSC_G2_IO3	PA6
	TSC_G2_IO4	PA7
3	TSC_G3_IO2	PB0
	TSC_G3_IO3	PB1
	TSC_G3_IO4	PB2
4	TSC_G4_IO1	PA9
	TSC_G4_IO2	PA10
	TSC_G4_IO3	PA11
	TSC_G4_IO4	PA12
5	TSC_G5_IO1	PB3
	TSC_G5_IO2	PB4
	TSC_G5_IO3	PB6
	TSC_G5_IO4	PB7

Table 6. No. of capacitive sensing channels available on STM32F042xx devices

Analog I/O group	Number of capacitive sensing channels				
	STM32F042Cx LQPF48 UQFPN48	STM32F042Tx WLCSP36	STM32F042Kx LQFP32 UQFPN32	STM32F042Gx UQFPN28	STM32F042Fx TSSOP20
G1	3	3	3	3	3
G2	3	3	3	3	3
G3	2	2	1 2	1	0
G4	3	3	3	1	1
G5	3	3	3	3	0
Number of capacitive sensing channels	14	14	13 14	11	7

3.12 Timers and watchdogs

The STM32F042xx devices include up to five general-purpose timers and an advanced control timer.

Table 7 compares the features of the advanced-control and general-purpose timers.

Table 7. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
Advanced control	TIM1	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	Yes
General purpose	TIM2	32-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
	TIM3	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
	TIM14	16-bit	Up	Any integer between 1 and 65536	No	1	No
	TIM16, TIM17	16-bit	Up	Any integer between 1 and 65536	Yes	1	Yes

3.12.1 Advanced-control timer (TIM1)

The advanced-control timer (TIM1) can be seen as a three-phase PWM multiplexed on six channels. It has complementary PWM outputs with programmable inserted dead times. It can also be seen as a complete general-purpose timer. The four independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes)
- One-pulse mode output

If configured as a standard 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0-100%).

The counter can be frozen in debug mode.

Many features are shared with those of the standard timers which have the same architecture. The advanced control timer can therefore work together with the other timers via the Timer Link feature for synchronization or event chaining.

3.12.2 General-purpose timers (TIM2..3, TIM14, 16, 17)

There are five synchronizable general-purpose timers embedded in the STM32F042xx devices (see *Table 7* for differences). Each general-purpose timer can be used to generate PWM outputs, or as simple time base.

TIM2, TIM3

STM32F042xx devices feature two synchronizable 4-channel general-purpose timers. TIM2 is based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler. TIM3 is based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. They feature 4 independent channels each for input capture/output compare, PWM or one-pulse mode output. This gives up to 12 input captures/output compares/PWMs on the largest packages.

The TIM2 and TIM3 general-purpose timers can work together or with the TIM1 advanced-control timer via the Timer Link feature for synchronization or event chaining.

TIM2 and TIM3 both have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

Their counters can be frozen in debug mode.

TIM14

This timer is based on a 16-bit auto-reload upcounter and a 16-bit prescaler.

TIM14 features one single channel for input capture/output compare, PWM or one-pulse mode output.

Its counter can be frozen in debug mode.

TIM16 and TIM17

Both timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler.

They each have a single channel for input capture/output compare, PWM or one-pulse mode output.

The TIM16 and TIM17 timers can work together via the Timer Link feature for synchronization or event chaining.

TIM16 and TIM17 have a complementary output with dead-time generation and independent DMA request generation.

Their counters can be frozen in debug mode.

3.12.3 Independent watchdog (IWDG)

The independent watchdog is based on an 8-bit prescaler and 12-bit downcounter with user-defined refresh window. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

3.12.4 System window watchdog (WWDG)

The system window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the APB clock (PCLK). It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.12.5 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source (HCLK or HCLK/8)

3.13 Real-time clock (RTC) and backup registers

The RTC and the 5 backup registers are supplied through a switch that takes power either on V_{DD} supply when present or through the V_{BAT} pin. The backup registers are five 32-bit registers used to store 20 bytes of user application data when V_{DD} power is not present. They are not reset by a system or power reset, or when the device wakes up from Standby mode.

The RTC is an independent BCD timer/counter. Its main features are the following:

- Calendar with subseconds, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- Automatically correction for 28, 29 (leap year), 30, and 31 day of the month.
- Programmable alarm with wake up from Stop and Standby mode capability.
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Digital calibration circuit with 1 ppm resolution, to compensate for quartz crystal inaccuracy.
- 2 anti-tamper detection pins with programmable filter. The MCU can be woken up from Stop and Standby modes on tamper event detection.
- Timestamp feature which can be used to save the calendar content. This function can triggered by an event on the timestamp pin, or by a tamper event. The MCU can be woken up from Stop and Standby modes on timestamp event detection.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.

The RTC clock sources can be:

- A 32.768 kHz external crystal
- A resonator or oscillator
- The internal low-power RC oscillator (typical frequency of 40 kHz)
- The high-speed external clock divided by 32

3.14 Inter-integrated circuit interfaces (I^2C)

The I^2C interface (I2C1) can operate in multimaster or slave modes. It can support Standard mode (up to 100 kbit/s), Fast mode (up to 400 kbit/s) and Fast Mode Plus (up to 1 Mbit/s) with 20 mA output drive on some I/Os.

It supports 7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (2 addresses, 1 with configurable mask). It also includes programmable analog and digital noise filters.

Table 8. Comparison of I2C analog and digital filters

	Analog filter	Digital filter
Pulse width of suppressed spikes	≥ 50 ns	Programmable length from 1 to 15 I2C peripheral clocks
Benefits	Available in Stop mode	1. Extra filtering capability vs. standard requirements. 2. Stable length
Drawbacks	Variations depending on temperature, voltage, process	Wakeup from Stop on address match is not available when digital filter is enabled.

In addition, I2C1 provides hardware support for SMBUS 2.0 and PMBUS 1.1: ARP capability, Host notify protocol, hardware CRC (PEC) generation/verification, timeouts verifications and ALERT protocol management. I2C1 also has a clock domain independent

from the CPU clock, allowing the I2C1 to wake up the MCU from Stop mode on address match.

The I2C interface can be served by the DMA controller.

Table 9. STM32F042xx I²C implementation

I2C features(1)	I2C1
7-bit addressing mode	X
10-bit addressing mode	X
Standard mode (up to 100 kbit/s)	X
Fast mode (up to 400 kbit/s)	X
Fast Mode Plus with 20mA output drive I/Os (up to 1 Mbit/s)	X
Independent clock	X
SMBus	X
Wakeup from STOP	X

1. X = supported.

3.15 Universal synchronous/asynchronous receiver transmitters (USART)

The device embeds up to two universal synchronous/asynchronous receiver transmitters (USART1 and USART2), which communicate at speeds of up to 6 Mbit/s.

They provide hardware management of the CTS, RTS and RS485 DE signals, multiprocessor communication mode, master synchronous communication and single-wire half-duplex communication mode. USART1 supports also SmartCard communication (ISO 7816), IrDA SIR ENDEC, LIN Master/Slave capability and auto baud rate feature, and has a clock domain independent from the CPU clock, allowing USART1 to wake up the MCU from Stop mode.

The USART interfaces can be served by the DMA controller.

Refer to *Table 10* for the differences between USART1 and USART2.

Table 10. STM32F042xx USART implementation

USART modes/features(1)	USART1	USART2
Hardware flow control for modem	X	X
Continuous communication using DMA	X	X
Multiprocessor communication	X	X
Synchronous mode	X	X
Smartcard mode	X	
Single-wire half-duplex communication	X	X
IrDA SIR ENDEC block	X	

Table 10. STM32F042xx USART implementation (continued)

USART modes/features(1)	USART1	USART2
LIN mode	X	
Dual clock domain and wakeup from Stop mode	X	
Receiver timeout interrupt	X	
Modbus communication	X	
Auto baud rate detection	X	
Driver Enable	X	X

1. X = supported.

3.16 Serial peripheral interface (SPI)/Inter-integrated sound interfaces (I^2S)

Up to two SPIs are able to communicate up to 18 Mbits/s in slave and master modes in full-duplex and half-duplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame size is configurable from 4 bits to 16 bits.

One standard I^2S interface (multiplexed with SPI1) supporting four different audio standards can operate as master or slave at half-duplex communication mode. It can be configured to transfer 16 and 24 or 32 bits with 16-bit or 32-bit data resolution and synchronized by a specific signal. Audio sampling frequency from 8 kHz up to 192 kHz can be set by an 8-bit programmable linear prescaler. When operating in master mode, it can output a clock for an external audio component at 256 times the sampling frequency.

Refer to *Table 11* for the differences between SPI1 and SPI2.

Table 11. STM32F042xx SPI/I2S implementation

SPI features(1)	SPI1	SPI2
Hardware CRC calculation	X	X
Rx/Tx FIFO	X	X
NSS pulse mode	X	X
I2S mode	X	
TI mode	X	X

1. X = supported.

3.17 High-definition multimedia interface (HDMI) - consumer electronics control (CEC)

The device embeds a HDMI-CEC controller that provides hardware support for the Consumer Electronics Control (CEC) protocol (Supplement 1 to the HDMI standard).

This protocol provides high-level control functions between all audiovisual products in an environment. It is specified to operate at low speeds with minimum processing and memory overhead. It has a clock domain independent from the CPU clock, allowing the HDMI_CEC controller to wakeup the MCU from Stop mode on data reception.

3.18 Controller area network (CAN)

The CAN is compliant with specifications 2.0A and B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has three transmit mailboxes, two receive FIFOs with 3 stages and 14 scalable filter banks.

3.19 Universal serial bus (USB)

The STM32F042xx embeds a full-speed USB device peripheral compliant with the USB specification version 2.0. The internal USB PHY supports USB FS signaling, embedded DP pull-up and also battery charging detection according to Battery Charging Specification Revision 1.2. The USB interface implements a full-speed (12 Mbit/s) function interface with added support for USB 2.0 Link Power Management. It has software-configurable endpoint setting with packet memory up-to 1 KB (the last 256 bytes are used for CAN peripheral if enabled) and suspend/resume support. It requires a precise 48 MHz clock which can be generated from the internal main PLL (the clock source must use an HSE crystal oscillator) or by the internal 48 MHz oscillator in automatic trimming mode. The synchronization for this oscillator can be taken from the USB data stream itself (SOF signalization) which allows crystal-less operation.

3.20 Clock recovery system (CRS)

The STM32F042xx embeds a special block which allows automatic trimming of the internal 48 MHz oscillator to guarantee its optimal accuracy over the whole device operational range. This automatic trimming is based on the external synchronization signal, which could be either derived from USB SOF signalization, from LSE oscillator, from an external signal on CRS_SYNC pin or generated by user software. For faster lock-in during startup it is also possible to combine automatic trimming with manual trimming action.

3.21 Serial wire debug port (SW-DP)

An ARM SW-DP interface is provided to allow a serial wire debugging tool to be connected to the MCU.

4 Pinouts and pin descriptions

Figure 3. LQFP48 48-pin package pinout (top view)

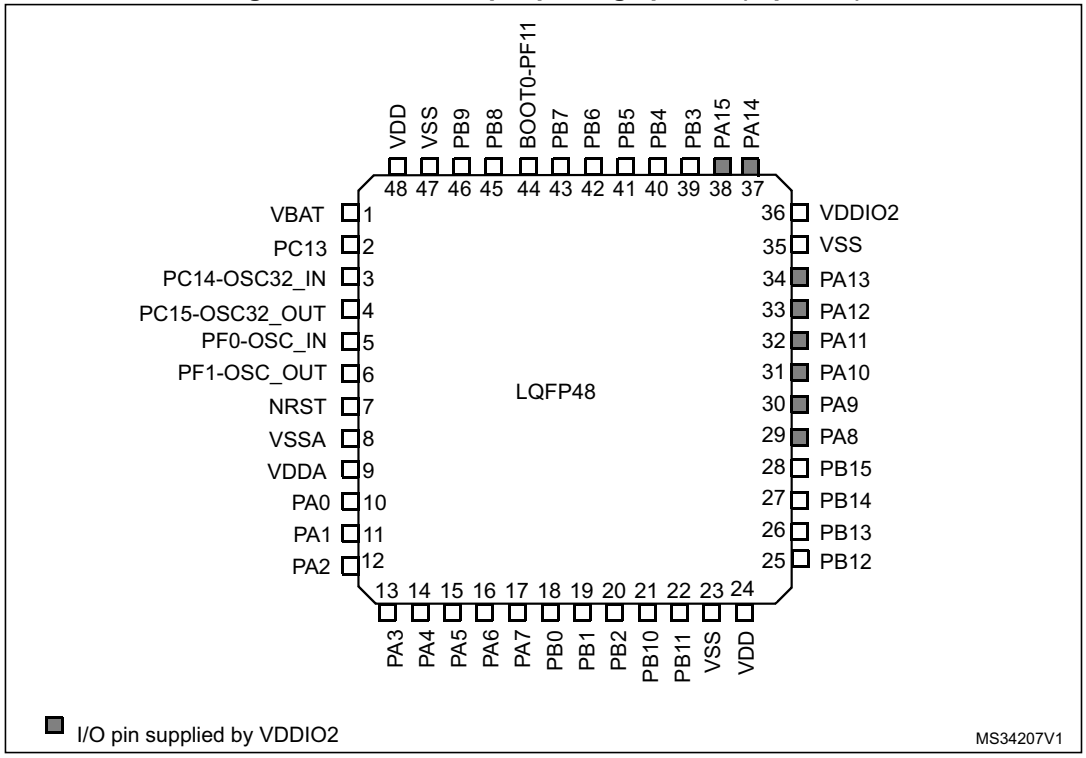


Figure 4. UFQFPN48 48-pin package pinout (top view)

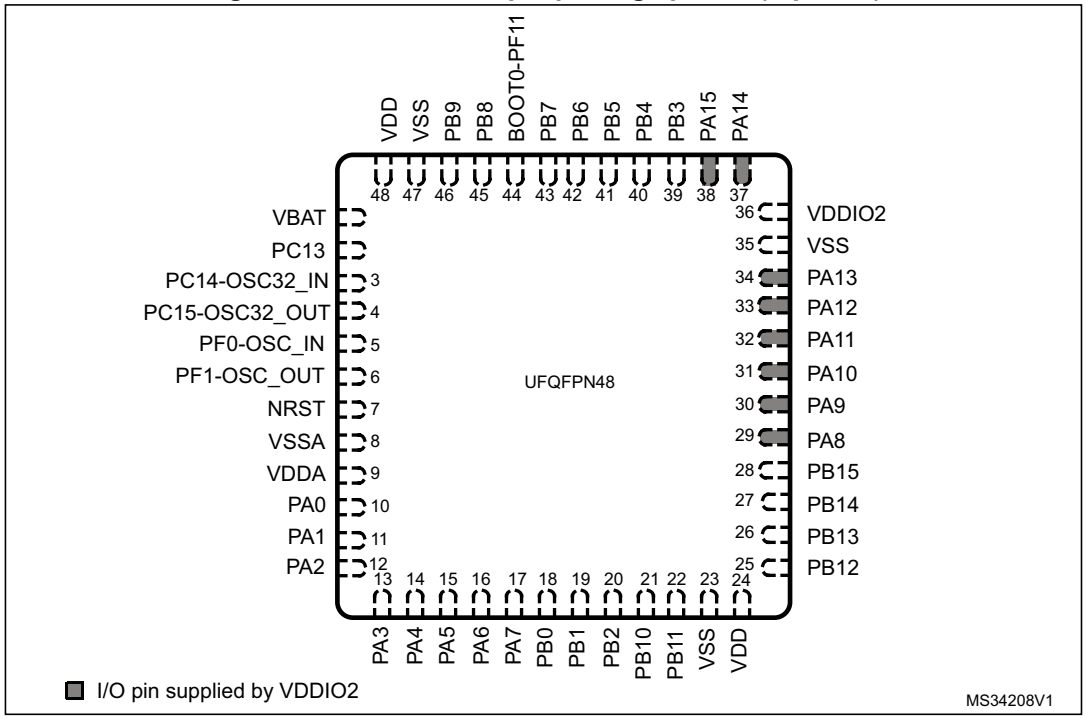


Figure 5. WLCSP36 36-pin package ball-out

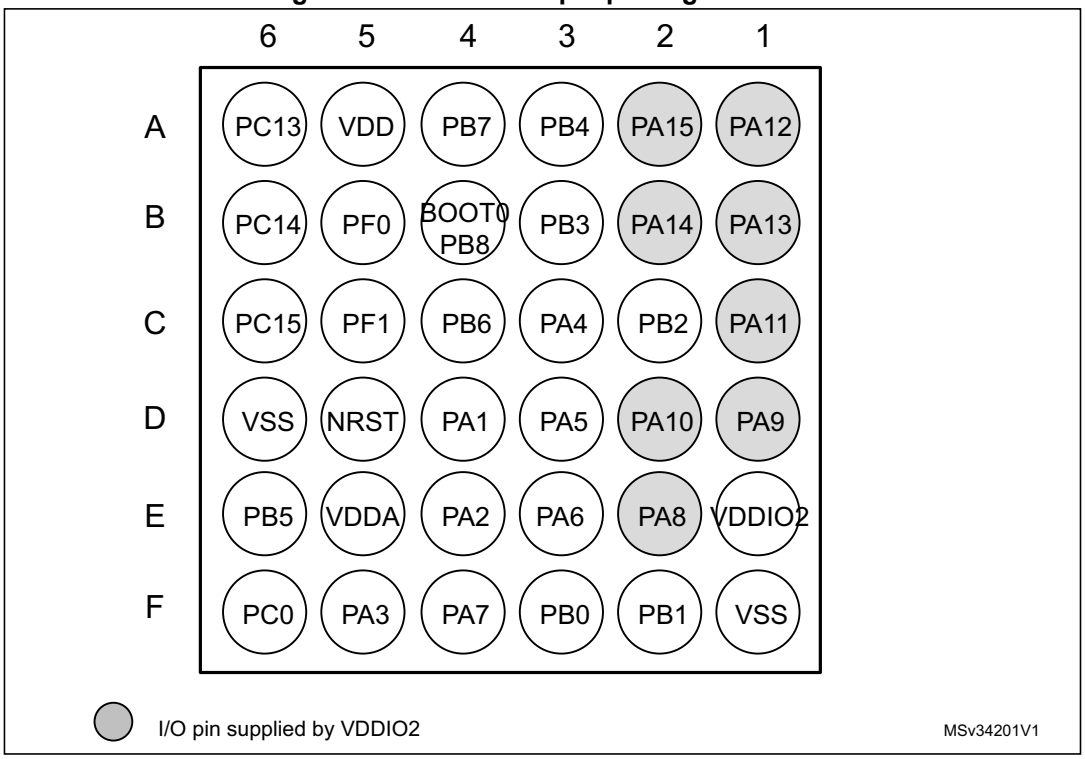


Figure 6. LQFP32 32-pin package pinout (top view)

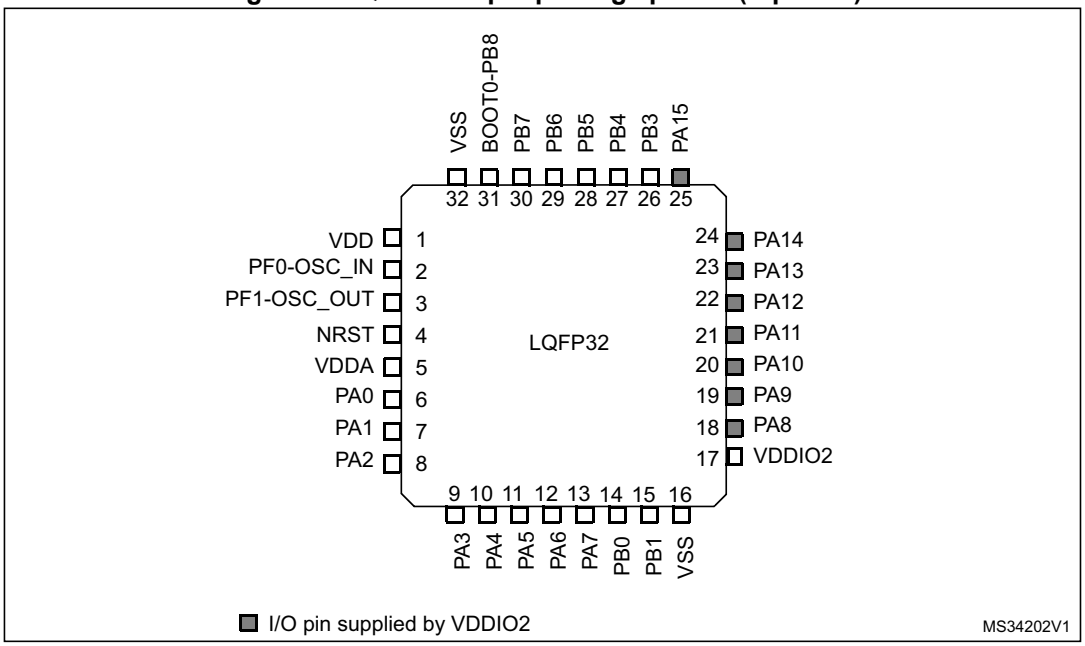


Figure 7. UFQFPN32 32-pin package pinout (top view)

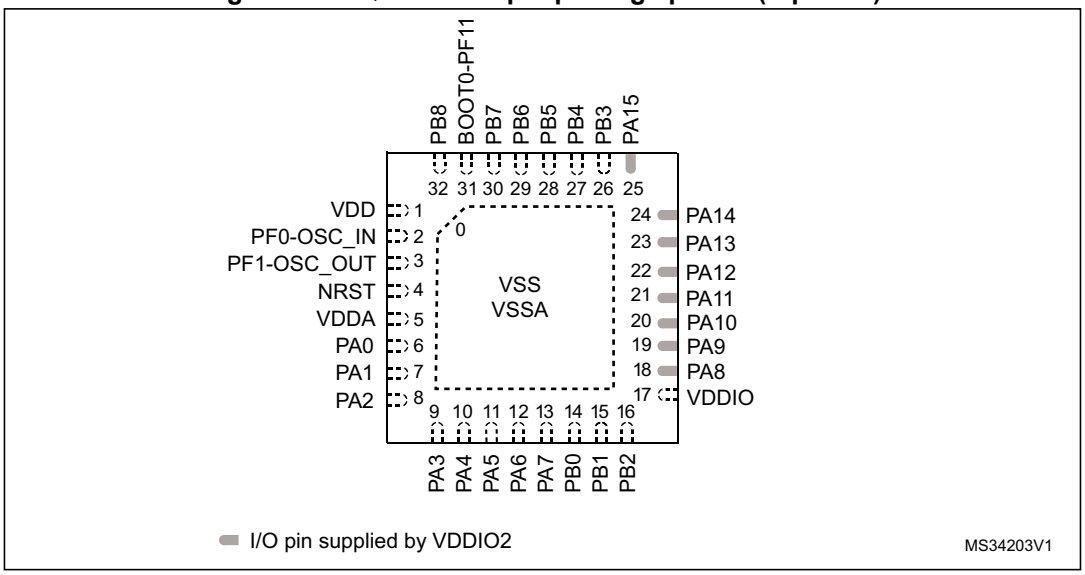
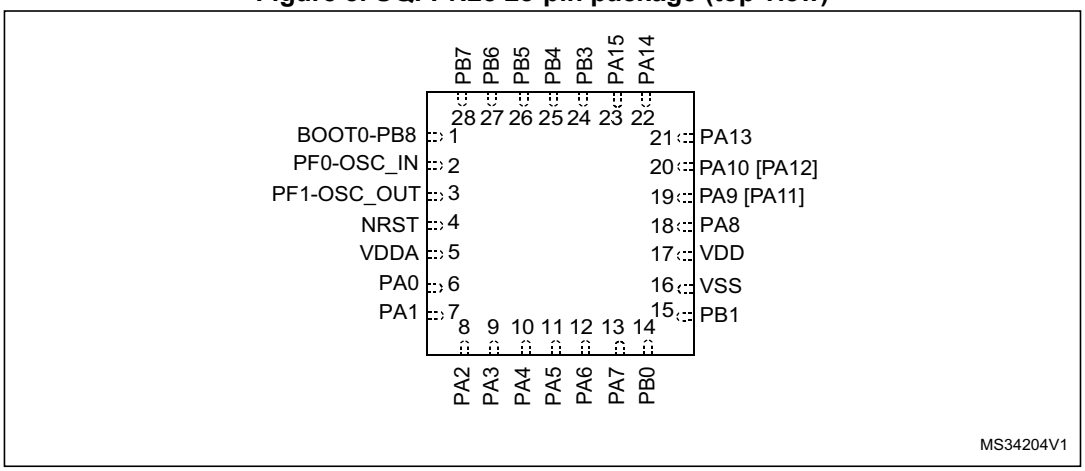
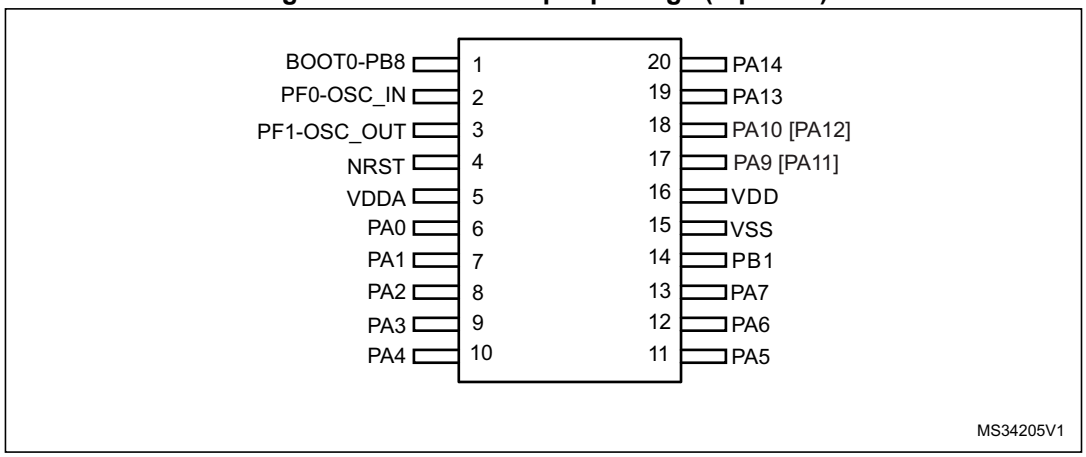


Figure 8. UQFPN28 28-pin package (top view)



1. Pin pair PA11/12 can be remapped instead of pin pair PA9/10 using the SYS_CTRL register.

Figure 9. TSSOP20 20-pin package (top view)



1. Pin pair PA11/12 can be remapped instead of pin pair PA9/10 using the SYS_CTRL register.

Table 12. Legend/abbreviations used in the pinout table

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type		S	Supply pin
		I	Input only pin
		I/O	Input / output pin
I/O structure		FT	5 V tolerant I/O
		FTf	5 V tolerant I/O, FM+ capable
		TTa	3.3 V tolerant I/O directly connected to ADC
		TC	Standard 3.3V I/O
		RST	Bidirectional reset pin with embedded weak pull-up resistor
Notes		Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset.	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

Table 13. STM32F042xx pin definitions

Pin numbers						Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP48/UFQFPN48	WLCSP36	LQFP32	UFQFPN32	UFQFPN28	TSSPOP20					Alternate function	Additional functions
1	-	-	-	-	-	VBAT	S			Backup power supply	
2	A6	-	-	-	-	PC13	I/O	TC	(1) (2)	-	WKUP2, RTC_TAMP1, RTC_TS, RTC_OUT
3	B6	-	-	-	-	PC14-OSC32_IN (PC14)	I/O	TC	(1) (2)	-	OSC32_IN
4	C6	-	-	-	-	PC15-OSC32_OUT (PC15)	I/O	TC	(1) (2)	-	OSC32_OUT
5	B5	2	2	2	2	PF0-OSC_IN (PF0)	I/O	FTf		CRS_ SYNC I2C1_SDA	OSC_IN

Table 13. STM32F042xx pin definitions (continued)

Pin numbers						Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP48/UFQFPN48	WLCSP36	LQFP32	UFQFPN32	UFQFPN28	TSSPOP20					Alternate function	Additional functions
6	C5	3	3	3	3	PF1-OSC_OUT (PF1)	I/O	FTf		I2C1_SCL	OSC_OUT
7	D5	4	4	4	4	NRST	I/O	RST		Device reset input / internal reset output (active low)	
8	D6	32	0	16	-	VSSA	S			Analog ground	
9	E5	5	5	5	5	VDDA	S			Analog power supply	
10	F6	6	6	6	6	PA0	I/O	TTa		USART2_CTS, TIM2_CH1_ETR, TSC_G1_IO1	RTC_ TAMP2, WKUP1, ADC_IN0,
11	D4	7	7	7	7	PA1	I/O	TTa		USART2_RTS, TIM2_CH2, TSC_G1_IO2, EVENTOUT	ADC_IN1
12	E4	8	8	8	8	PA2	I/O	TTa		USART2_TX, TIM2_CH3, TSC_G1_IO3	ADC_IN2, WKUP4
13	F5	9	9	9	9	PA3	I/O	TTa		USART2_RX, TIM2_CH4, TSC_G1_IO4	ADC_IN3
14	C3	10	10	10	10	PA4	I/O	TTa		SPI1_NSS, I2S1_WS, TIM14_CH1, TSC_G2_IO1, USART2_CK USB_NOE	ADC_IN4
15	D3	11	11	11	11	PA5	I/O	TTa		SPI1_SCK, I2S1_CK, CEC, TIM2_CH1_ETR, TSC_G2_IO2	ADC_IN5
16	E3	12	12	12	12	PA6	I/O	TTa		SPI1_MISO, I2S1_MCK, TIM3_CH1, TIM1_BKIN, TIM16_CH1, TSC_G2_IO3, EVENTOUT	ADC_IN6

Table 13. STM32F042xx pin definitions (continued)

Pin numbers						Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP48/UFQFPN48	WLCSP36	LQFP32	UFQFPN32	UFQFPN28	TSSPOP20					Alternate function	Additional functions
17	F4	13	13	13	13	PA7	I/O	TTa		SPI1_MOSI, I2S1_SD, TIM3_CH2, TIM14_CH1, TIM1_CH1N, TIM17_CH1, TSC_G2_IO4, EVENTOUT	ADC_IN7
18	F3	14	14	14	-	PB0	I/O	TTa		TIM3_CH3, TIM1_CH2N, TSC_G3_IO2, EVENTOUT	ADC_IN8
19	F2	15	15	15	14	PB1	I/O	TTa		TIM3_CH4, TIM14_CH1, TIM1_CH3N, TSC_G3_IO3	ADC_IN9
20	C2	-	16	-	-	PB2	I/O	FT		TSC_G3_IO4	-
21	-	-	-	-	-	PB10	I/O	FT		SPI2_SCK, CEC, TSC_SYNC, TIM2_CH3, I2C1_SCL	-
22	-	-	-	-	-	PB11	I/O	FT		TIM2_CH4, EVENTOUT, I2C1_SDA	-
23	F1	16	0	15	15	VSS	S			Ground	
24	-	-	-	17	16	VDD	S			Digital power supply	
25	-	-	-	-	-	PB12	I/O	FT		TIM1_BKIN, SPI2_NSS, EVENTOUT	-
26	-	-	-	-	-	PB13	I/O	FTf		SPI2_SCK, I2S2_CK, TIM1_CH1N, I2C1_SCL	-
27	-	-	-	-	-	PB14	I/O	FTf		SPI2_MISO, I2S2_MCK, TIM1_CH2N, I2C1_SDA	-
28	-	-	-	-	-	PB15	I/O	FT		SPI2_MOSI, TIM1_CH3N	WKUP7, RTC_REFIN
29	E2	18	18	18	-	PA8	I/O	FT	(3)	USART1_CK, TIM1_CH1, EVENTOUT, MCO, CRS_SYNC	-

Table 13. STM32F042xx pin definitions (continued)

Pin numbers						Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP48/UFQFPN48	WLCSP36	LQFP32	UFQFPN32	UFQFPN28	TSSPOP20					Alternate function	Additional functions
30	D1	19	19	19	17	PA9	I/O	FTf	(3)	USART1_TX, TIM1_CH2, TSC_G4_IO1, I2C1_SCL	-
31	D2	20	20	20	18	PA10	I/O	FTf	(3)	USART1_RX, TIM1_CH3, TIM17_BKIN, TSC_G4_IO2, I2C1_SDA	-
32	C1	21	21	19(4)	17(4)	PA11	I/O	FTf	(3)	CAN_RX, USART1_CTS, TIM1_CH4, COMP1_OUT, TSC_G4_IO3, EVENTOUT, I2C1_SCL	USB_DM
33	A1	22	22	20(4)	18(4)	PA12	I/O	FTf	(3)	CAN_TX,USART1_RTS, TIM1_ETR, TSC_G4_IO4, EVENTOUT, I2C1_SDA	USB_DP
34	B1	23	23	21	19	PA13	I/O	FT	(3) (5)	IR_OUT, SWDIO USB_NOE	-
35	-	-	-	-	-	VSS	S			Ground	
36	E1	17	17	-	-	VDDIO2	S			Digital power supply	
37	B2	24	24	22	20	PA14	I/O	FTf	(3) (5)	USART2_TX, SWCLK	-
38	A2	25	25	23	-	PA15	I/O	FTf	(3)	SPI1_NSS, I2S1_WS, USART2_RX, TIM2_CH1_ETR, EVENTOUT, USB_NOE	-
39	B3	26	26	24	-	PB3	I/O	FT		SPI1_SCK, I2S1_CK, TIM2_CH2, TSC_G5_IO1, EVENTOUT	-

Table 13. STM32F042xx pin definitions (continued)

Pin numbers						Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP48/UFQFPN48	WLCSP36	LQFP32	UFQFPN32	UFQFPN28	TSSPOP20					Alternate function	Additional functions
40	A3	27	27	25	-	PB4	I/O	FT		SPI1_MISO, I2S1_MCK, TIM17_BKIN, TIM3_CH1, TSC_G5_IO2, EVENTOUT	-
41	-	28	28	26	-	PB5	I/O	FT		SPI1_MOSI, I2S1_SD, I2C1_SMBA, TIM16_BKIN, TIM3_CH2	WKUP6
42	C4	29	29	27	-	PB6	I/O	FTf		I2C1_SCL, USART1_TX, TIM16_CH1N, TSC_G5_I03	-
43	A4	30	30	28	-	PB7	I/O	FTf		I2C1_SDA, USART1_RX, USART4_CTS, TIM17_CH1N, TSC_G5_IO4	-
44	-	-	31	-	-	PF11 BOOT0	I/O	FT		Boot memory selection	-
-	B4	31	-	1	1	PB8 BOOT0	I/O	FTf		I2C1_SCL, CEC, TIM16_CH1, TSC_SYNC, CAN_RX Boot memory selection	-
45	-	-	32	-	-	PB8	I/O	FTf		I2C1_SCL, CEC, TIM16_CH1, TSC_SYNC, CAN_RX	-
46	-	-	-	-	-	PB9	I/O	FTf		SPI2_NSS, I2S2_WS, I2C1_SDA, IR_OUT, TIM17_CH1, EVENTOUT, CAN_TX	-
47	-	32	0	-	-	VSS	S			Ground	
48	A5	1	1	-	-	VDD	S			Digital power supply	

1. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited:
   - The speed should not exceed 2 MHz with a maximum load of 30 pF.
   - These GPIOs must not be used as current sources (e.g. to drive an LED).

2. After the first RTC domain power-up, PC13, PC14 and PC15 operate as GPIOs. Their function then depends on the content of the RTC registers which are not reset by the system reset. For details on how to manage these GPIOs, refer to the RTC domain and RTC register descriptions in the reference manual.
3. PA8, PA9, PA10, PA11, PA12, PA13, PA14 and PA15 I/Os are supplied by VDDIO2.
4. Pin pair PA11/12 can be remapped instead of pin pair PA9/10 using SYS_CTRL register.
5. After reset, these pins are configured as SWDIO and SWCLK alternate functions, and the internal pull-up on the SWDIO pin and the internal pull-down on the SWCLK pin are activated.

Table 14. Alternate functions selected through GPIOA_AFR registers for port A

Pin name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA0		USART2_CTS	TIM2_CH1_ETR	TSC_G1_IO1				
PA1	EVENTOUT	USART2_RTS	TIM2_CH2	TSC_G1_IO2				
PA2		USART2_TX	TIM2_CH3	TSC_G1_IO3				
PA3		USART2_RX	TIM2_CH4	TSC_G1_IO4				
PA4	SPI1_NSS, I2S1_WS	USART2_CK	USB_NOE	TSC_G2_IO1	TIM14_CH1			
PA5	SPI1_SCK, I2S1_CK	CEC	TIM2_CH1_ETR	TSC_G2_IO2				
PA6	SPI1_MISO, I2S1_MCK	TIM3_CH1	TIM1_BKIN	TSC_G2_IO3		TIM16_CH1	EVENTOUT	
PA7	SPI1_MOSI, I2S1_SD	TIM3_CH2	TIM1_CH1N	TSC_G2_IO4	TIM14_CH1	TIM17_CH1	EVENTOUT	
PA8	MCO	USART1_CK	TIM1_CH1	EVENTOUT	CRS_SYNC			
PA9		USART1_TX	TIM1_CH2	TSC_G4_IO1	I2C1_SCL	MCO		
PA10	TIM17_BKIN	USART1_RX	TIM1_CH3	TSC_G4_IO2	I2C1_SDA			
PA11	EVENTOUT	USART1_CTS	TIM1_CH4	TSC_G4_IO3	CAN_RX	I2C1_SCL		
PA12	EVENTOUT	USART1_RTS	TIM1_ETR	TSC_G4_IO4	CAN_TX	I2C1_SDA		
PA13	SWDIO	IR_OUT	USB_NOE					
PA14	SWCLK	USART2_TX						
PA15	SPI1_NSS, I2S1_WS	USART2_RX	TIM2_CH1_ETR	EVENTOUT		USB_NOE		

Table 15. Alternate functions selected through GPIOB_AFR registers for port B

Pin name	AF0	AF1	AF2	AF3	AF4	AF5
PB0	EVENTOUT	TIM3_CH3	TIM1_CH2N	TSC_G3_IO2		
PB1	TIM14_CH1	TIM3_CH4	TIM1_CH3N	TSC_G3_IO3		
PB2				TSC_G3_IO4		
PB3	SPI1_SCK, I2S1_CK	EVENTOUT	TIM2_CH2	TSC_G5_IO1		
PB4	SPI1_MISO, I2S1_MCK	TIM3_CH1	EVENTOUT	TSC_G5_IO2		TIM17_BKIN
PB5	SPI1_MOSI, I2S1_SD	TIM3_CH2	TIM16_BKIN	I2C1_SMBA		
PB6	USART1_TX	I2C1_SCL	TIM16_CH1N	TSC_G5_IO3		
PB7	USART1_RX	I2C1_SDA	TIM17_CH1N	TSC_G5_IO4		
PB8	CEC	I2C1_SCL	TIM16_CH1	TSC_SYNC	CAN_RX	
PB9	IR_OUT	I2C1_SDA	TIM17_CH1	EVENTOUT	CAN_TX	SPI2_NSS
PB10	CEC		TIM2_CH3	TSC_SYNC		SPI2_SCK
PB11	EVENTOUT		TIM2_CH4			
PB12	SPI2_NSS	EVENTOUT	TIM1_BKIN			
PB13	SPI2_SCK		TIM1_CH1N			I2C2_SCL
PB14	SPI2_MISO		TIM1_CH2N			I2C2_SDA
PB15	SPI2_MOSI		TIM1_CH3N			

Table 16. Alternate functions selected through GPIOF_AFR registers for port F

Pin name	AF0	AF1
PF0	CRS_SYNC	I2C1_SDA
PF1		I2C1_SCL

5 Memory mapping

Figure 10. STM32F042xx memory map

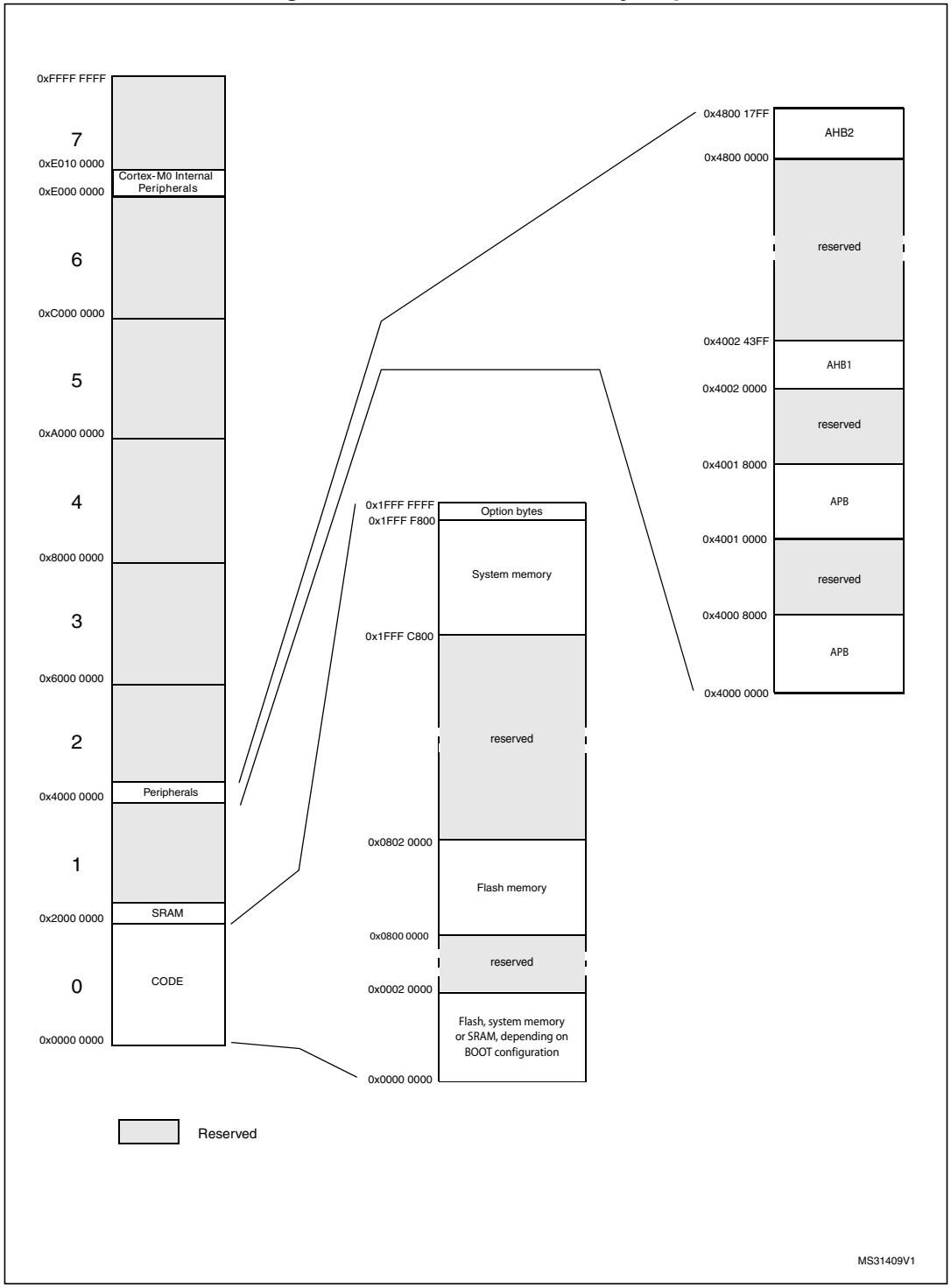


Table 17. STM32F042xx peripheral register boundary addresses

Bus	Boundary address	Size	Peripheral
	0x4800 1800 - 0x5FFF FFFF	~384 MB	Reserved
AHB2	0x4800 1400 - 0x4800 17FF	1 KB	GPIOF
	0x4800 0C00 - 0x4800 13FF	2 KB	Reserved
	0x4800 0800 - 0x4800 0BFF	1 KB	GPIOC
	0x4800 0400 - 0x4800 07FF	1 KB	GPIOB
	0x4800 0000 - 0x4800 03FF	1 KB	GPIOA
	0x4002 4400 - 0x47FF FFFF	~128 MB	Reserved
AHB1	0x4002 4000 - 0x4002 43FF	1 KB	TSC
	0x4002 3400 - 0x4002 3FFF	3 KB	Reserved
	0x4002 3000 - 0x4002 33FF	1 KB	CRC
	0x4002 2400 - 0x4002 2FFF	3 KB	Reserved
	0x4002 2000 - 0x4002 23FF	1 KB	FLASH Interface
	0x4002 1400 - 0x4002 1FFF	3 KB	Reserved
	0x4002 1000 - 0x4002 13FF	1 KB	RCC
	0x4002 0400 - 0x4002 0FFF	3 KB	Reserved
	0x4002 0000 - 0x4002 03FF	1 KB	DMA
	0x4001 8000 - 0x4001 FFFF	32 KB	Reserved
APB	0x4001 5C00 - 0x4001 7FFF	9 KB	Reserved
	0x4001 5800 - 0x4001 5BFF	1 KB	DBGMCU
	0x4001 4C00 - 0x4001 57FF	3 KB	Reserved
	0x4001 4800 - 0x4001 4BFF	1 KB	TIM17
	0x4001 4400 - 0x4001 47FF	1 KB	TIM16
	0x4001 3C00 - 0x4001 43FF	2 KB	Reserved
	0x4001 3800 - 0x4001 3BFF	1 KB	USART1
	0x4001 3400 - 0x4001 37FF	1 KB	Reserved
	0x4001 3000 - 0x4001 33FF	1 KB	SPI1/I2S1
	0x4001 2C00 - 0x4001 2FFF	1 KB	TIM1
	0x4001 2800 - 0x4001 2BFF	1 KB	Reserved
	0x4001 2400 - 0x4001 27FF	1 KB	ADC
	0x4001 0800 - 0x4001 23FF	7 KB	Reserved
	0x4001 0400 - 0x4001 07FF	1 KB	EXTI
	0x4001 0000 - 0x4001 03FF	1 KB	SYSCFG + COMP
	0x4000 8000 - 0x4000 FFFF	32 KB	Reserved

Table 17. STM32F042xx peripheral register boundary addresses (continued)

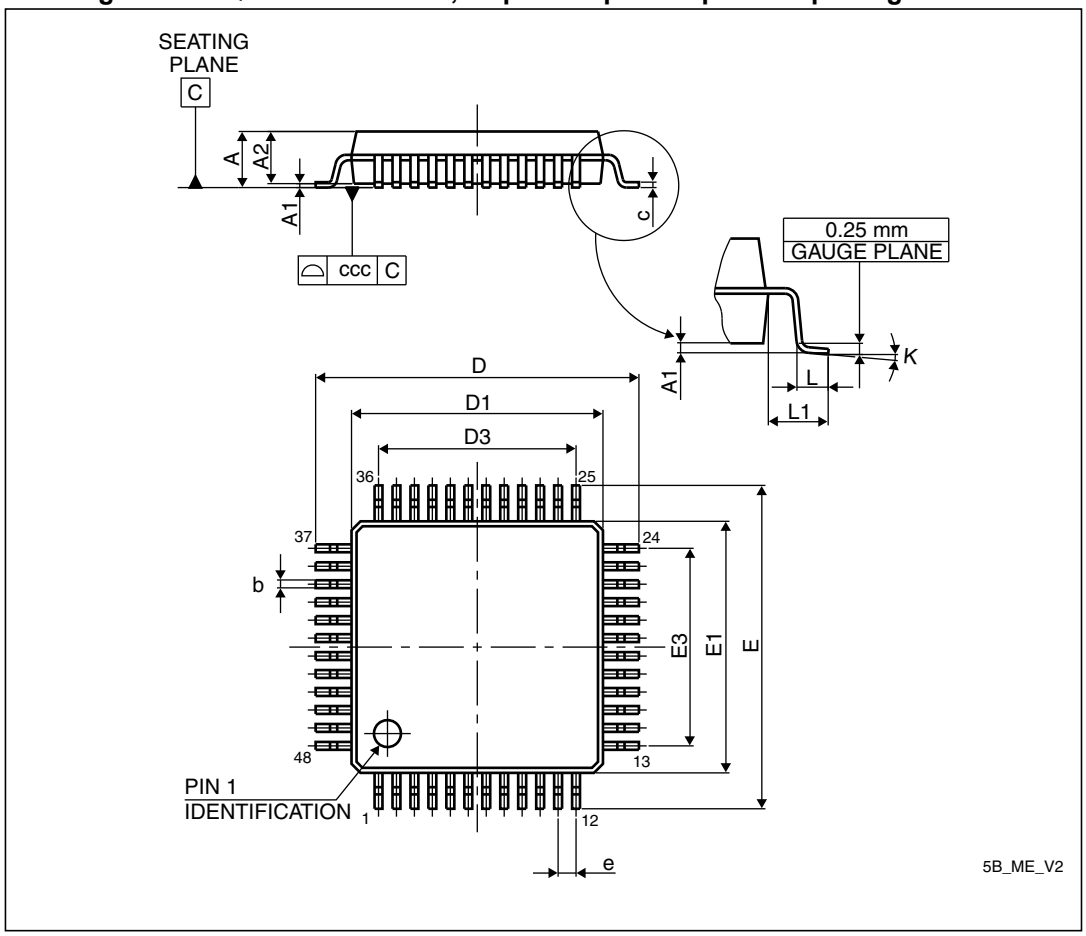
Bus	Boundary address	Size	Peripheral
APB	0x4000 7C00 - 0x4000 7FFF	1 KB	Reserved
	0x4000 7800 - 0x4000 7BFF	1 KB	CEC
	0x4000 7400 - 0x4000 77FF	1 KB	Reserved
	0x4000 7000 - 0x4000 73FF	1 KB	PWR
	0x4000 6C00 - 0x4000 6FFF	1 KB	CRS
	0x4000 6800 - 0x4000 6BFF0	1 KB	Reserved
	0x4000 6400 - 0x4000 67FF	1 KB	BxCAN
	0x4000 6000 - 0x4000 63FF	1 KB	USB/CAN RAM
	0x4000 5C00 - 0x4000 5FFF	1 KB	USB
	0x4000 5800 - 0x4000 5BFF	1 KB	Reserved
	0x4000 5400 - 0x4000 57FF	1 KB	I2C1
	0x4000 4800 - 0x4000 53FF	3 KB	Reserved
	0x4000 4400 - 0x4000 47FF	1 KB	USART2
	0x4000 3C00 - 0x4000 43FF	2 KB	Reserved
	0x4000 3800 - 0x4000 3BFF	1 KB	SPI2
	0x4000 3400 - 0x4000 37FF	1 KB	Reserved
	0x4000 3000 - 0x4000 33FF	1 KB	IWDG
	0x4000 2C00 - 0x4000 2FFF	1 KB	WWDG
	0x4000 2800 - 0x4000 2BFF	1 KB	RTC
	0x4000 2400 - 0x4000 27FF	1 KB	Reserved
	0x4000 2000 - 0x4000 23FF	1 KB	TIM14
	0x4000 0800 - 0x4000 1FFF	6 KB	Reserved
	0x4000 0400 - 0x4000 07FF	1 KB	TIM3
	0x4000 0000 - 0x4000 03FF	1 KB	TIM2

6 Package characteristics

6.1 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 11. LQFP48 – 7 x 7 mm, 48 pin low-profile quad flat package outline



1. Drawing is not to scale.

Table 18. LQFP48 – 7 x 7 mm low-profile quad flat package mechanical data

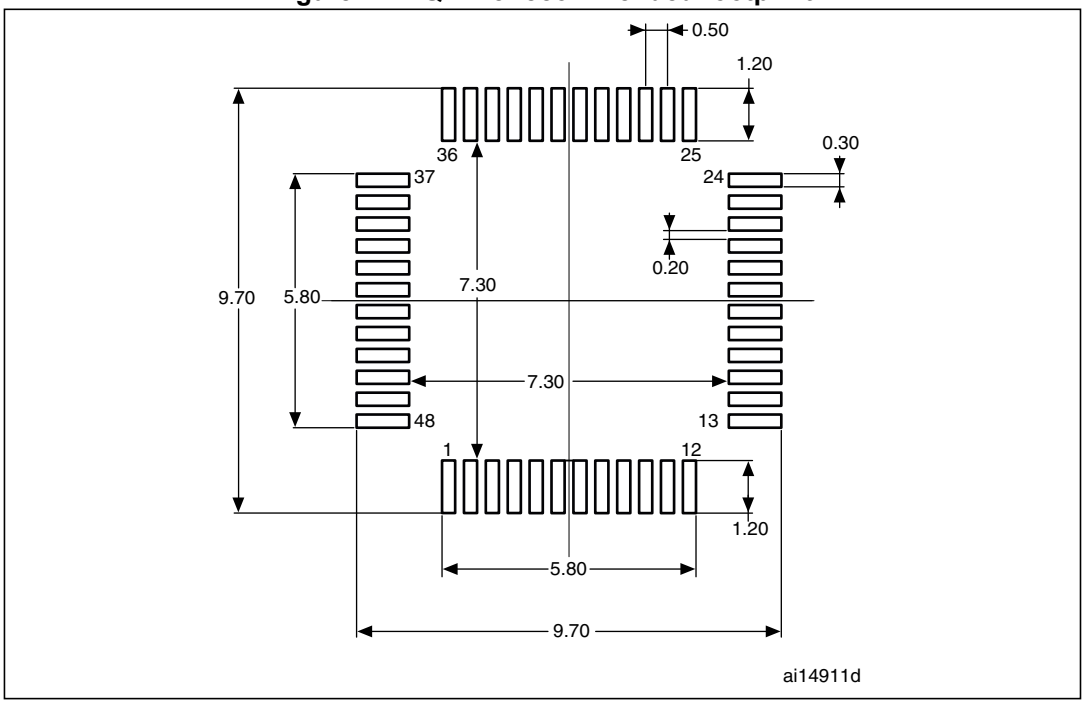
Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A		-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106

Table 18. LQFP48 – 7 x 7 mm low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031
K	0°	3.5°	7°	0°	3.5°	7°

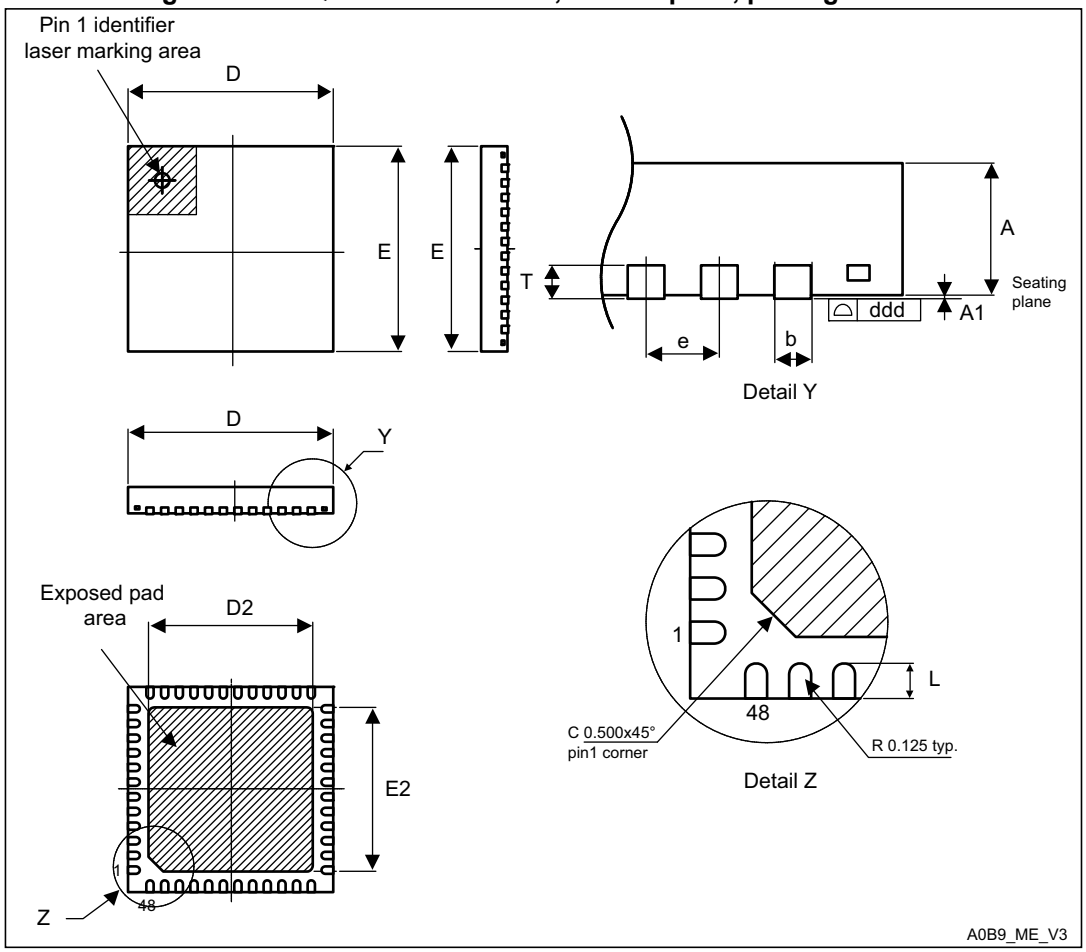
1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 12. LQFP48 recommended footprint



1. Dimensions are in millimeters.

Figure 13. UFQFPN48 – 7 x 7 mm, 0.5 mm pitch, package outline



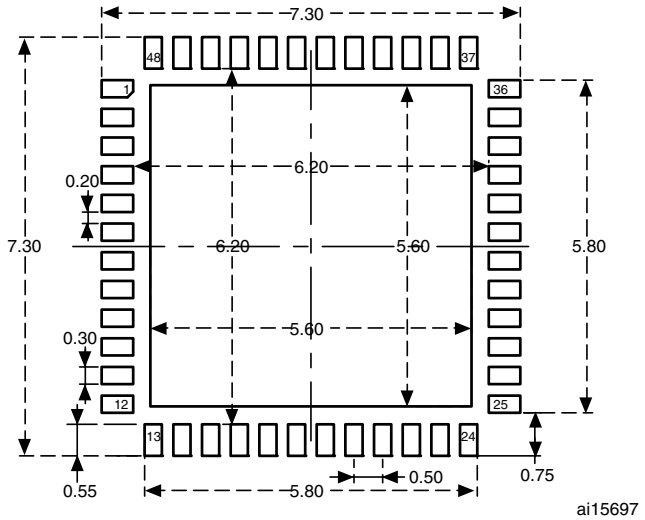
1. Drawing is not to scale.
2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN package. It is recommended to connect and solder this back-side pad to PCB ground.

Table 19. UFQFPN48 – 7 x 7 mm, 0.5 mm pitch, package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
D	6.900	7.000	7.100	0.2717	0.2756	0.2795
E	6.900	7.000	7.100	0.2717	0.2756	0.2795
D2	5.500	5.600	5.700	0.2165	0.2205	0.2244
E2	5.500	5.600	5.700	0.2165	0.2205	0.2244
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
T	-	0.152	-	-	0.0060	-
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
e	-	0.500	-	-	0.0197	-

1. Values in inches are converted from mm and rounded to 4 decimal digits.

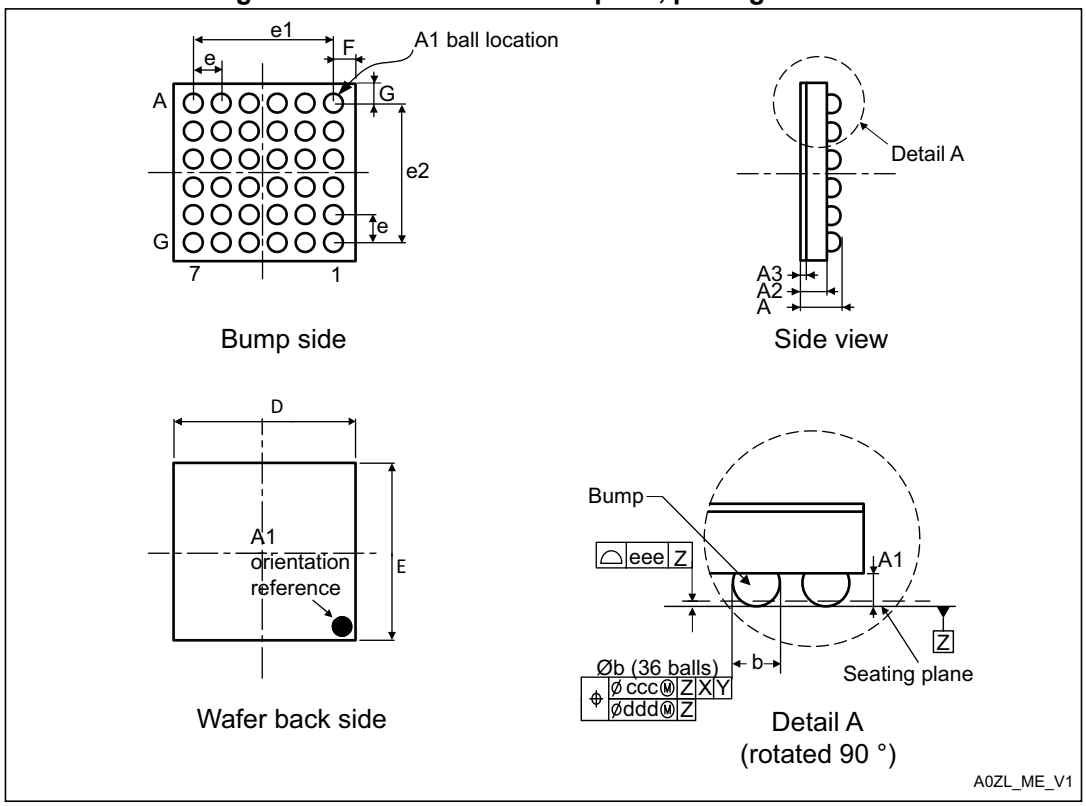
Figure 14. UFQFPN48 recommended footprint



1. Dimensions are in millimeters.

1. Samples marked “ES” are to be considered as “Engineering Samples”: i.e. they are intended to be sent to customer for electrical compatibility evaluation and may be used to start customer qualification where specifically authorized by ST in writing. In no event ST will be liable for any customer usage in production. Only if ST has authorized in writing the customer qualification Engineering Samples can be used for reliability qualification trials.

Figure 15. WLCSP36 - 0.4 mm pitch, package outline



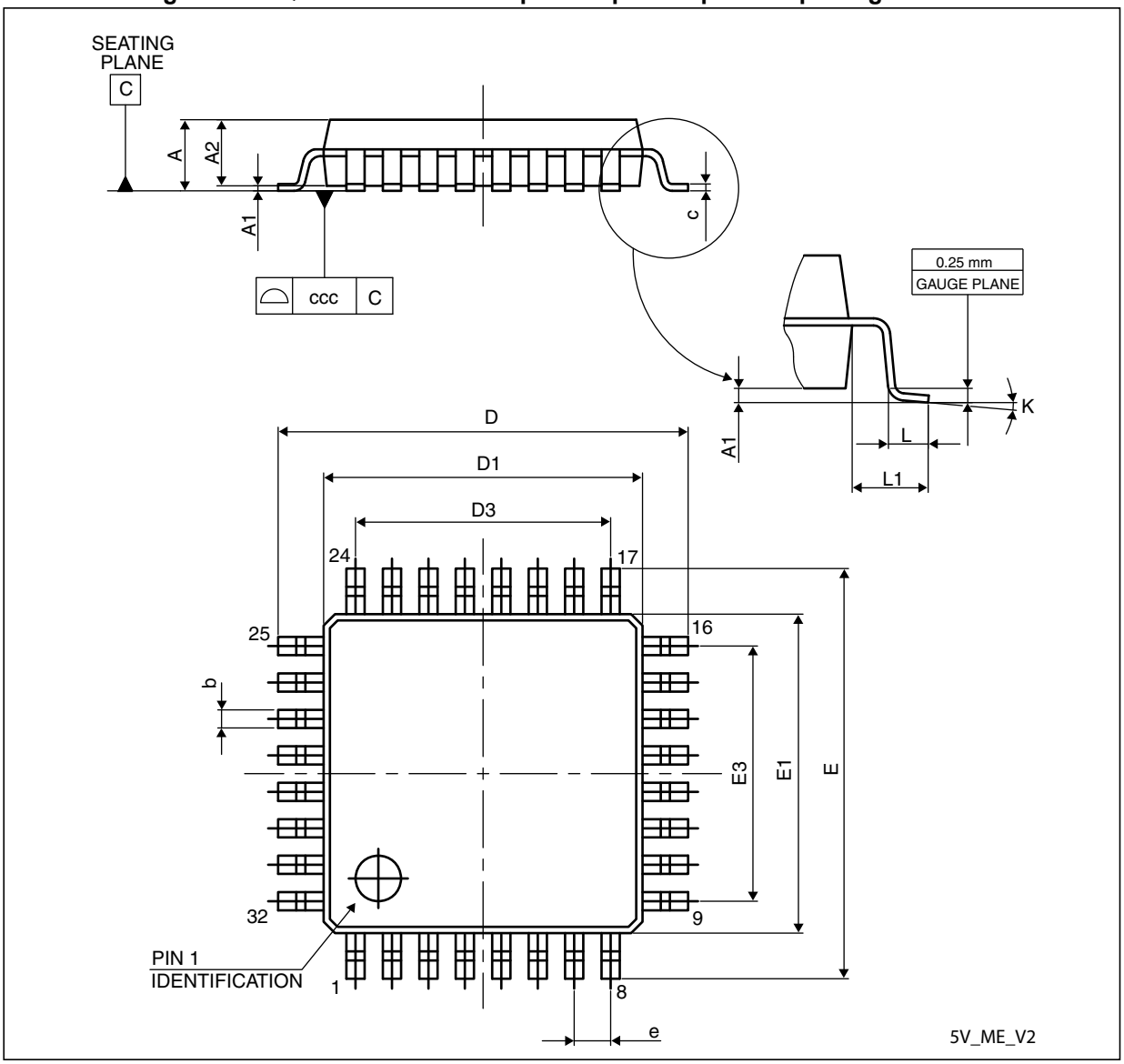
1. Drawing is not to scale.

Table 20. WLCSP36, 0.4 mm pitch, package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.555	0.525	0.585	0.0219	0.0207	0.0230
A1	0.175	-	-	0.0069	-	-
A2	0.380	-	-	0.0150	-	-
A3[2]	0.025	-	-	0.0010	-	-
b[3]	0.250	0.220	0.280	0.0098	0.0087	0.0110
D	2.605	2.570	2.640	0.1026	0.1012	0.1039
E	2.703	2.668	2.738	0.1064	0.1050	0.1078
e	0.400	-	-	0.0157	-	-
e1	2.000	-	-	0.0787	-	-
e2	2.000	-	-	0.0787	-	-
F	0.3025	-	-	0.0119	-	-
G	0.2825	-	-	0.0111	-	-
ccc	0.100	-	-	0.0039	-	-
ddd	0.050	-	-	0.0020	-	-
eee	0.050	-	-	0.0020	-	-

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Back side coating
3. Dimension is measured at the maximum bump diameter parallel to primary datum Z.

Figure 16. LQFP32 – 7 x 7mm 32-pin low-profile quad flat package outline



1. Drawing is not to scale.

Table 21. LQFP32 – 7 x 7mm 32-pin low-profile quad flat package mechanical data

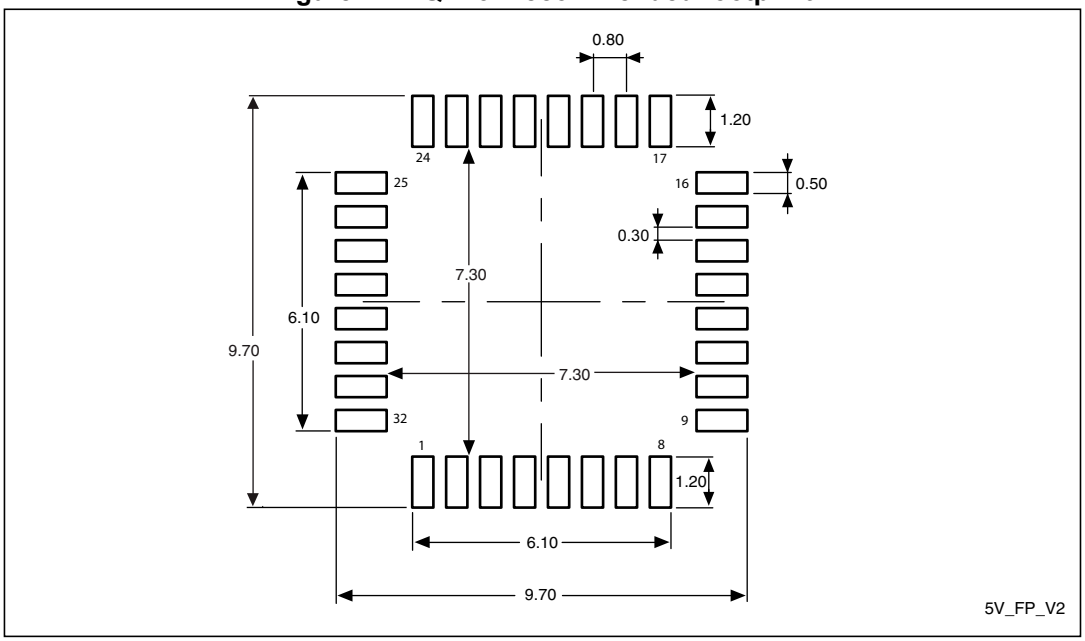
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.300	0.370	0.450	0.0118	0.0146	0.0177
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622

Table 21. LQFP32 – 7 x 7mm 32-pin low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.600	-	-	0.2205	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.600	-	-	0.2205	-
e	-	0.800	-	-	0.0315	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc	-	-	0.100	-	-	0.0039

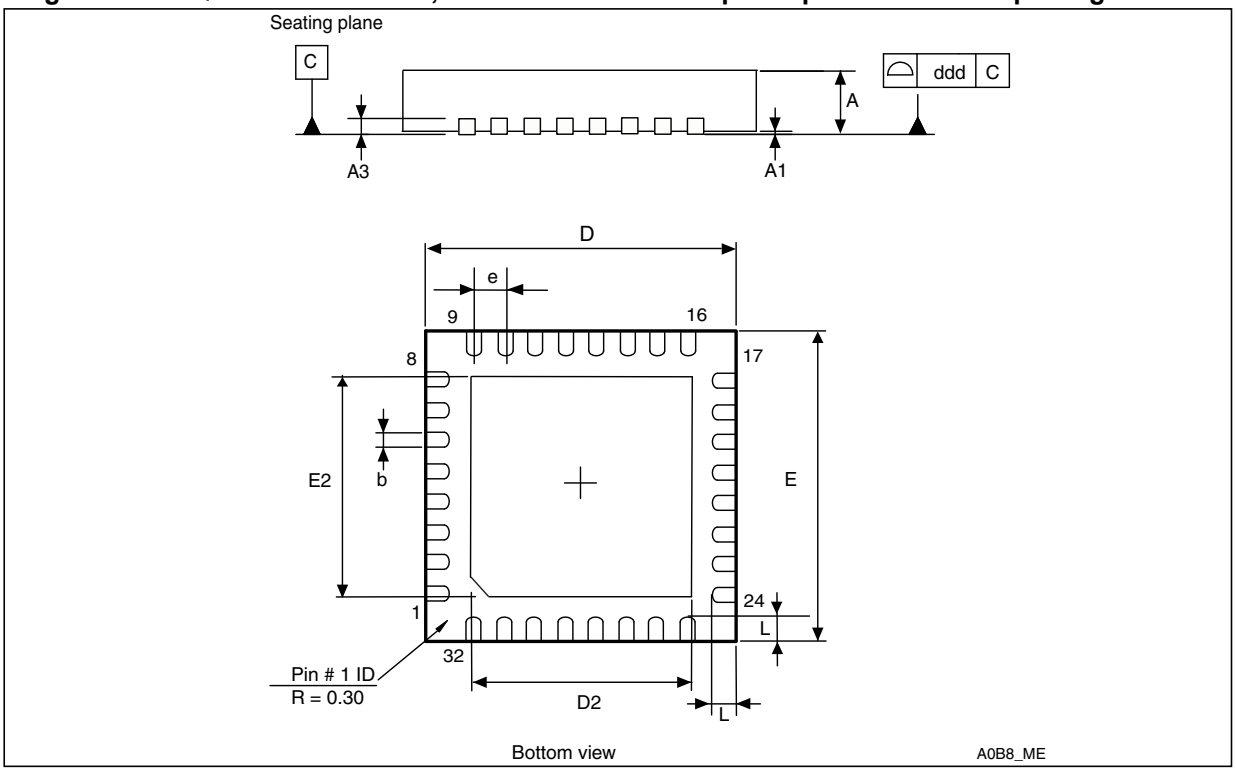
1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 17. LQFP32 recommended footprint



1. Drawing is not to scale.
2. Dimensions are in millimeters.

Figure 18. UFQFPN32 - 5 x 5 mm, 32-lead ultra thin fine pitch quad flat no-lead package outline



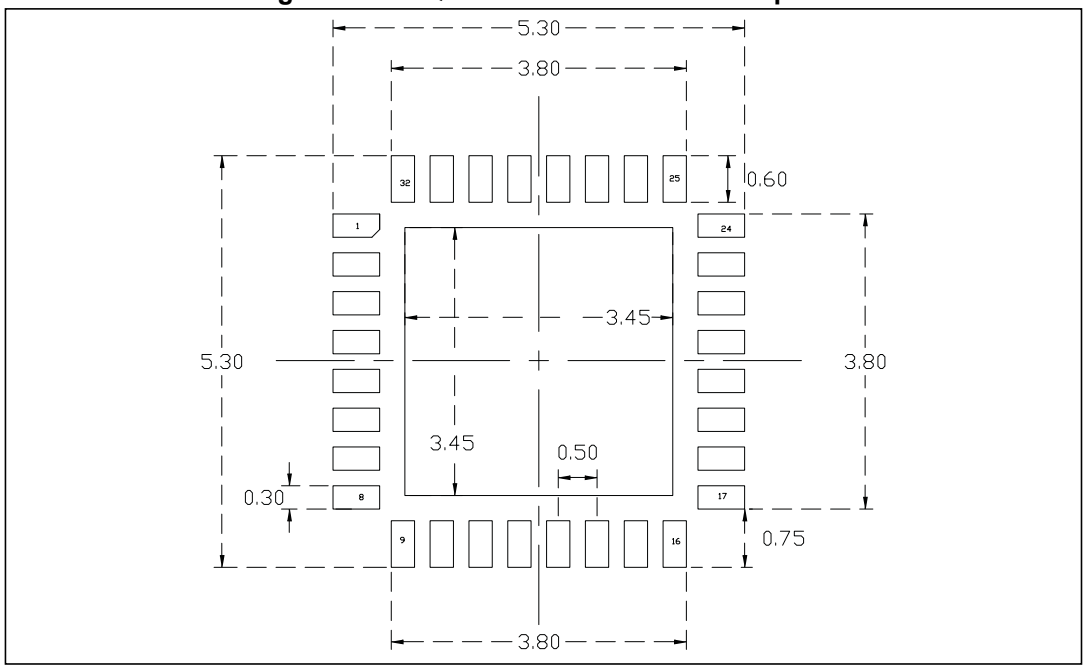
1. Drawing is not to scale.
2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN package. This pad is used for the device ground and must be connected. It is referred to as pin 0 in *Table 12: Legend/abbreviations used in the pinout table*.

Table 22. UFQFPN32 – 5 x 5 mm, 32-lead ultra thin fine pitch quad flat no-lead package mechanical data

Dim.	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.5	0.55	0.6	0.0197	0.0217	0.0236
A1	0.00	0.02	0.05	0	0.0008	0.0020
A3	-	0.152	-	-	0.006	-
b	0.18	0.23	0.28	0.0071	0.0091	0.0110
D	4.90	5.00	5.10	0.1929	0.1969	0.2008
D2	-	3.50	-	-	0.1378	-
E	4.90	5.00	5.10	0.1929	0.1969	0.2008
E2	3.40	3.50	3.60	0.1339	0.1378	0.1417
e	-	0.500	-	-	0.0197	-
L	0.30	0.40	0.50	0.0118	0.0157	0.0197
ddd		0.08			0.0031	

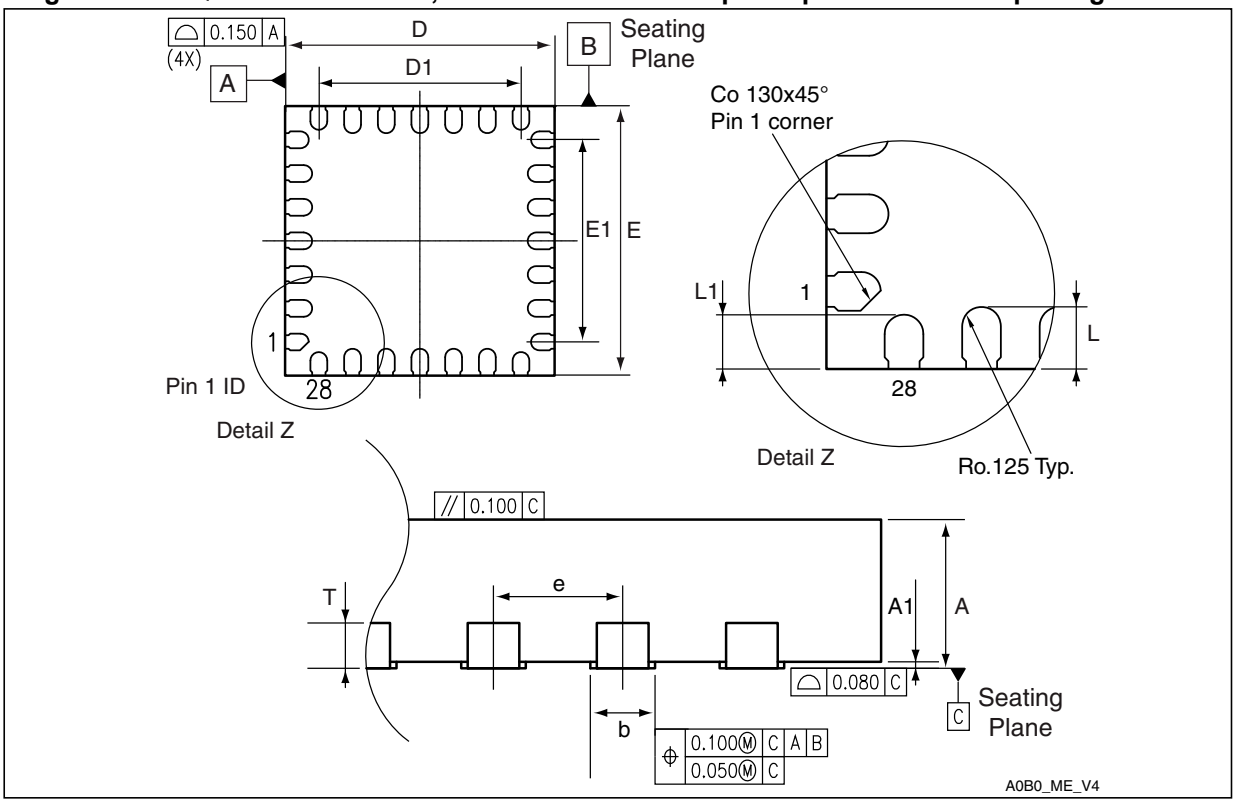
1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 19. UFQFPN32 recommended footprint



1. Drawing is not to scale.
2. Dimensions are in millimeters.

Figure 20. UFQFPN28 - 4 x 4 mm, 28-lead ultra thin fine pitch quad flat no-lead package outline



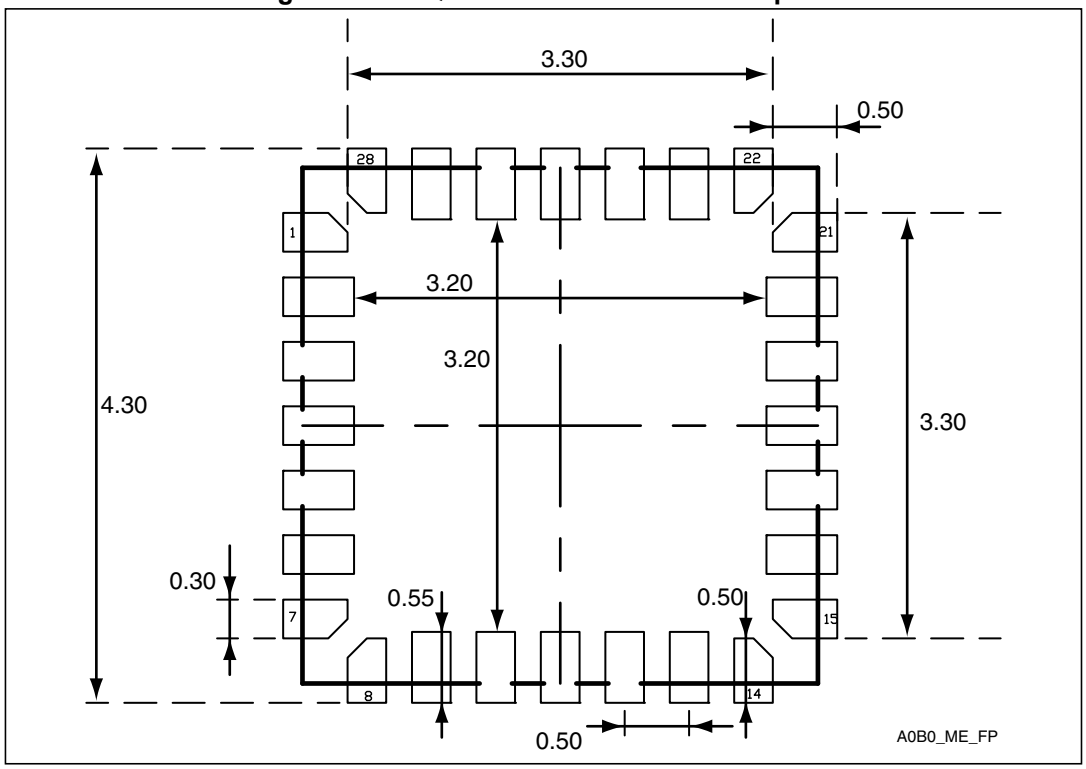
1. Drawing is not to scale.
2. Dimensions are in millimeters.
3. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.

Table 23. UFQFPN28 – 4 x 4 mm, 28-lead ultra thin fine pitch quad flat no-lead package mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	0.5	0.55	0.6	0.0197	0.0217	0.0236
A1	-0.05	0	0.05	-0.002	0	0.002
D	3.9	4	4.1	0.1535	0.1575	0.1614
D1	2.9	3	3.1	0.1142	0.1181	0.122
E	3.9	4	4.1	0.1535	0.1575	0.1614
E1	2.9	3	3.1	0.1142	0.1181	0.122
L	0.3	0.4	0.5	0.0118	0.0157	0.0197
L1	0.25	0.35	0.45	0.0098	0.0138	0.0177
T	-	0.152	-	-	0.006	-
b	0.2	0.25	0.3	0.0079	0.0098	0.0118
e	-	0.5	-	-	0.0197	-

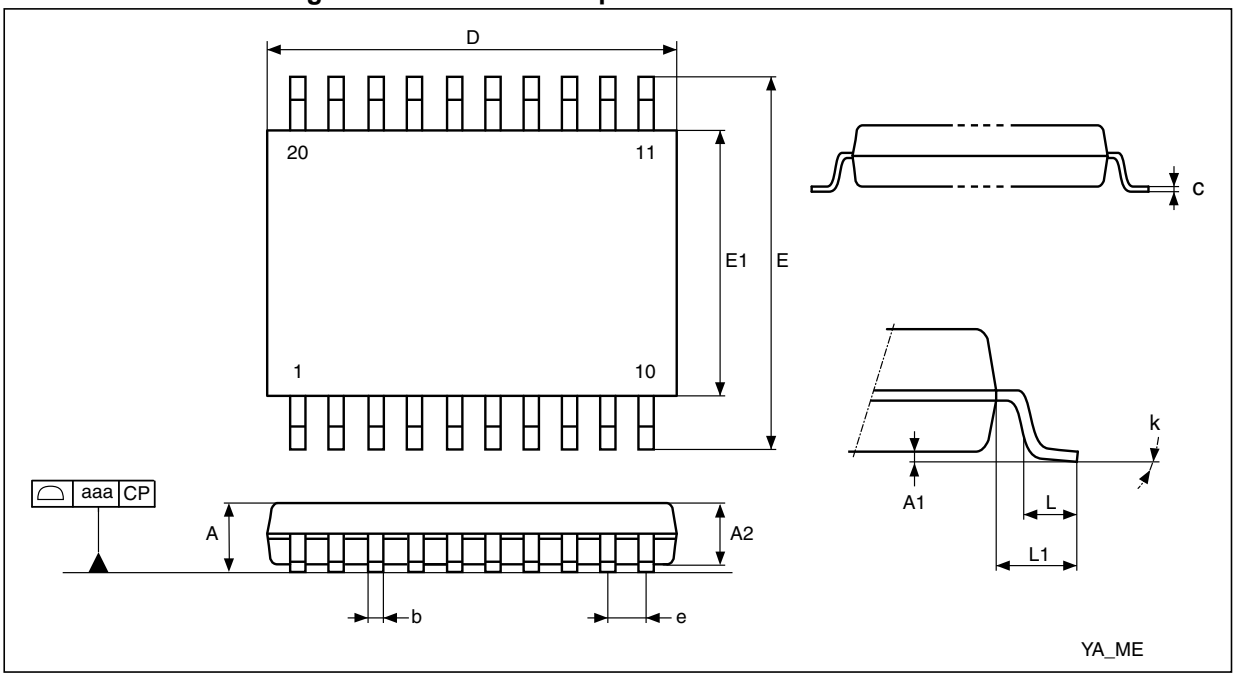
1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 21. UFQFPN28 recommended footprint



1. Dimensions are in millimeters
2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.

Figure 22. TSSOP20 - 20-pin thin shrink small outline



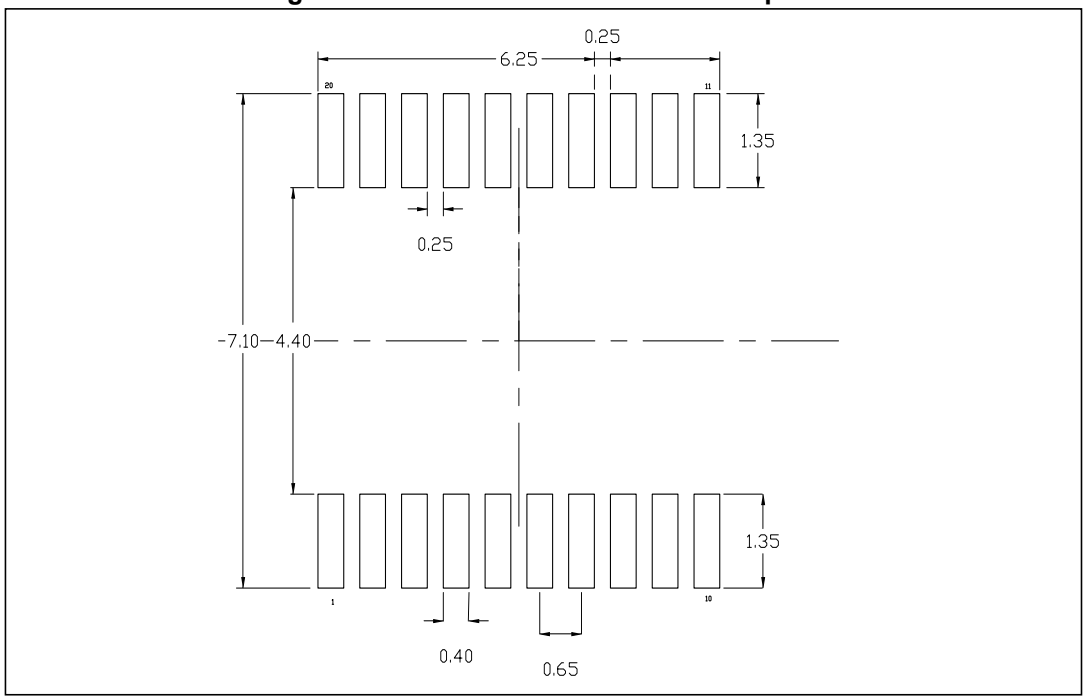
1. Drawing is not to scale.

Table 24. TSSOP20 – 20-pin thin shrink small outline package mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	
A		-	1.2	-	-	0.0472
A1	0.05	-	0.15	0.002	-	0.0059
A2	0.8	1	1.05	0.0315	0.0394	0.0413
b	0.19		0.3	0.0075	-	0.0118
c	0.09		0.2	0.0035	-	0.0079
D(2)	6.4	6.5	6.6	0.252	0.2559	0.2598
E	6.2	6.4	6.6	0.2441	0.252	0.2598
E1(3)	4.3	4.4	4.5	0.1693	0.1732	0.1772
e	-	0.65	-	-	0.0256	-
L	0.45	0.6	0.75	0.0177	0.0236	0.0295
L1	-	1	-	-	0.0394	-
k	0.0°	-	8.0°	0.0°	-	8.0°
aaa	-	-	0.1	-	-	0.0039

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.
3. Dimension “E1” does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25mm per side.

Figure 23. TSSOP20 recommended footprint



1. Dimensions are in millimeters

7 Part numbering

For a list of available options (memory, package, and so on) or for further information on any aspect of this device, please contact your nearest ST sales office.

Table 25. Ordering information scheme

Example: STM32 F 042 C 6 T 6 x

Device family

STM32 = ARM-based 32-bit microcontroller

Product type

F = General-purpose

Sub-family

042 = STM32F042xx

Pin count

F = 20 pins
G = 28 pins
K = 32 pins
T = 36 pins
C = 48 pins

Code size

4 = 16 Kbytes of Flash memory
6 = 32 Kbytes of Flash memory

Package

P = TSSOP
T = LQFPP
U = UFQFPN
Y = WLCSP

Temperature range

6 = –40 to 85 °C
7 = –40 to 105 °C

Options

xxx = programmed parts
TR = tape and reel

8 Revision history

Table 26. Document revision history

Date	Revision	Changes
13-Jan-2014	1	Initial release.

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST’s terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST’S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

ST PRODUCTS ARE NOT DESIGNED OR AUTHORIZED FOR USE IN: (A) SAFETY CRITICAL APPLICATIONS SUCH AS LIFE SUPPORTING, ACTIVE IMPLANTED DEVICES OR SYSTEMS WITH PRODUCT FUNCTIONAL SAFETY REQUIREMENTS; (B) AERONAUTIC APPLICATIONS; (C) AUTOMOTIVE APPLICATIONS OR ENVIRONMENTS, AND/OR (D) AEROSPACE APPLICATIONS OR ENVIRONMENTS. WHERE ST PRODUCTS ARE NOT DESIGNED FOR SUCH USE, THE PURCHASER SHALL USE PRODUCTS AT PURCHASER’S SOLE RISK, EVEN IF ST HAS BEEN INFORMED IN WRITING OF SUCH USAGE, UNLESS A PRODUCT IS EXPRESSLY DESIGNATED BY ST AS BEING INTENDED FOR “AUTOMOTIVE, AUTOMOTIVE SAFETY OR MEDICAL” INDUSTRY DOMAINS ACCORDING TO ST PRODUCT DESIGN SPECIFICATIONS. PRODUCTS FORMALLY ESCC, QML OR JAN QUALIFIED ARE DEEMED SUITABLE FOR USE IN AEROSPACE BY THE CORRESPONDING GOVERNMENTAL AGENCY.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.
Information in this document supersedes and replaces all information previously supplied.
The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com