

ESD PROTECTED, HIGH-SPEED USB 2.0 (480-Mbps) 1:2 MULTIPLEXER/DEMULTIPLEXER SWITCH WITH SINGLE ENABLE

Check for Samples: [TS3USB221A-Q1](#)

FEATURES

- Qualified for Automotive Applications
- V_{CC} Operation at 2.5 V to 3.3 V
- V_{IO} Accepts Signals Up to 5.5 V
- 1.8-V Compatible Control-Pin Inputs
- Low-Power Mode When \overline{OE} Is Disabled (1 μ A)
- $r_{ON} = 16 \Omega$ Maximum
- $\Delta r_{ON} = 0.2 \Omega$ Typical
- $C_{io(on)} = 6$ pF Typical
- Low Power Consumption (30 μ A Maximum)
- High Bandwidth (900 MHz Typical)
- ESD Performance Tested Per JESD 22
 - 7000-V Human-Body Model (A114-B, Class II)
 - 1000-V Charged-Device Model (C101)
- ESD Performance I/O to GND
 - 12-kV Human-Body Model

APPLICATIONS

- Routes Signals for USB 1.0, 1.1, and 2.0



DESCRIPTION

The TS3USB221A is a high-bandwidth switch specially designed for the switching of high-speed USB 2.0 signals in handset and consumer applications, such as cell phones, digital cameras, and notebooks with hubs or controllers with limited USB I/Os. The wide bandwidth (900 MHz) of this switch allows signals to pass with minimum edge and phase distortion. The device multiplexes differential outputs from a USB host device to one of two corresponding outputs. The switch is bidirectional and offers little or no attenuation of the high-speed signals at the outputs. It is designed for low bit-to-bit skew and high channel-to-channel noise isolation, and is compatible with various standards, such as high-speed USB 2.0 (480 Mbps).

The TS3USB221A integrates ESD protection cells on all pins, is available in a tiny μ QFN package (2.0 mm \times 1.5 mm) and is characterized over the free air temperature range from -40°C to 125°C .

ORDERING INFORMATION⁽¹⁾

T_A	PACKAGE ⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 125°C	QFN – RSE	Reel of 3000	TS3USB221AQRSERQ1	OFW

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
- (2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.



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PIN DESCRIPTION

NAME	DESCRIPTION
\overline{OE}	Bus-switch enable
S	Select input
D	Bus A
nD	Bus B

TRUTH TABLE

S	\overline{OE}	FUNCTION
X	H	Disconnect
L	L	D = 1D
H	L	D = 2D

BLOCK DIAGRAM

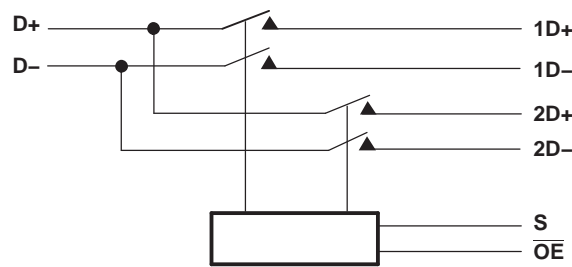
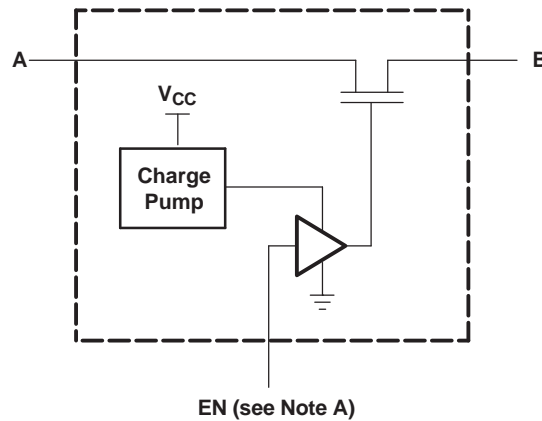


Figure 1. SIMPLIFIED SCHEMATIC, EACH FET SWITCH (SW)



A. EN is the internal enable signal applied to the switch.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		-0.5	4.6	V
V _{IN}	Control input voltage range ^{(2) (3)}		-0.5	7	V
V _{I/O}	Switch I/O voltage range ^{(2) (3) (4)}		-0.5	7	V
I _{IK}	Control input clamp current	V _{IN} < 0		-50	mA
I _{I/O} K	I/O port clamp current	V _{I/O} < 0		-50	mA
I _{I/O}	ON-state switch current ⁽⁵⁾			±120	mA
	Continuous current through V _{CC} or GND			±100	mA
T _{stg}	Storage temperature range		-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to ground, unless otherwise specified.
- (3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (4) V_I and V_O are used to denote specific conditions for V_{I/O}.
- (5) I_I and I_O are used to denote specific conditions for I_{I/O}.

PACKAGE THERMAL IMPEDANCE

over operating free-air temperature range (unless otherwise noted)

				UNIT
θ _{JA}	Package thermal impedance ⁽¹⁾	RSE package	243	°C/W
θ _{JC}	Junction-to-case thermal resistance		84	°C/W

- (1) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
V _{CC}	Supply voltage		2.3	3.6	V
V _{IH}	High-level control input voltage	V _{CC} = 2.3 V to 2.7 V	0.46 × V _{CC}		V
		V _{CC} = 2.7 V to 3.6 V	0.46 × V _{CC}		
V _{IL}	Low-level control input voltage	V _{CC} = 2.3 V to 2.7 V		0.25 × V _{CC}	V
		V _{CC} = 2.7 V to 3.6 V		0.25 × V _{CC}	
V _{I/O}	Data input/output voltage		0	5.5	V
T _A	Operating free-air temperature		-40	125	°C

ELECTRICAL CHARACTERISTICS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP ⁽²⁾	MAX	UNIT	
V _{IK}		V _{CC} = 3.6 V, 2.7 V, I _I = -18 mA				-1.8	V	
I _{IN}	Control inputs	V _{CC} = 3.6 V, 2.7 V, 0 V, V _{IN} = 0 V to 3.6 V				±1	μA	
I _{OZ} ⁽³⁾		V _{CC} = 3.6 V, 2.7 V, V _O = 0 V to 5.25 V, V _I = 0 V, V _{IN} = V _{CC} or GND, Switch OFF				±1	μA	
I _{I(OFF)}	V _{CC} = 0 V	V _{I/O} = 0 V to 5.25 V				±2	μA	
		V _{I/O} = 0 V to 3.6 V				±2		
		V _{I/O} = 0 V to 2.7 V				±1		
I _{CC}		V _{CC} = 3.6 V, 2.7 V, V _{IN} = V _{CC} or GND, I _{I/O} = 0 V, Switch ON or OFF				30	μA	
I _{CC} (low power mode)		V _{CC} = 3.6 V, 2.7 V, V _{IN} = V _{CC} or GND, Switch disabled, \overline{OE} in high state				1	μA	
ΔI _{CC} ⁽⁴⁾	Control inputs	One input at 1.8 V, Other inputs at V _{CC} or GND	V _{CC} = 3.6 V				20	μA
			V _{CC} = 2.7 V				0.5	
C _{in}	Control inputs	V _{CC} = 3.3 V, 2.5 V, V _{IN} = V _{CC} or 0 V			1.5	2.5	pF	
C _{io(OFF)}		V _{CC} = 3.3 V, 2.5 V, V _{I/O} = V _{CC} or 0 V, Switch OFF			3.5	5	pF	
C _{io(ON)}		V _{CC} = 3.3 V, 2.5 V, V _{I/O} = V _{CC} or 0 V, Switch ON			6	7.5	pF	
r _{ON} ⁽⁵⁾	V _{CC} = 3 V, 2.3 V	V _I = 0 V, I _O = 30 mA		T _A = 25°C	3	6	Ω	
		V _I = 2.4 V, I _O = -15 mA			3.4	6		
		V _I = 0 V, I _O = 30 mA		T _A = 125°C	6	10		
		V _I = 2.4 V, I _O = -15 mA			10	16		
Δr _{ON}	V _{CC} = 3 V, 2.3 V	V _I = 0 V, I _O = 30 mA			0.2		Ω	
		V _I = 1.7 V, I _O = -15 mA			0.2			
r _{ON(flat)}	V _{CC} = 3 V, 2.3 V	V _I = 0 V, I _O = 30 mA			1		Ω	
		V _I = 1.7 V, I _O = -15 mA			1			

- (1) V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.
- (2) All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.
- (3) For I/O ports, the parameter I_{OZ} includes the input leakage current.
- (4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.
- (5) Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

DYNAMIC ELECTRICAL CHARACTERISTICS

over operating range, T_A = -40°C to 125°C, V_{CC} = 3.3 V ±10%, GND = 0 V

PARAMETER		TEST CONDITIONS	TYP	UNIT
X _{TALK}	Crosstalk	R _L = 50 , f = 250 MHz	-40	dB
O _{IRR}	OFF isolation	R _L = 50 , f = 250 MHz	-41	dB
BW	Bandwidth (-3 dB)	R _L = 50	0.9	GHz

DYNAMIC ELECTRICAL CHARACTERISTICS

over operating range, $T_A = -40^{\circ}\text{C}$ to 125°C , $V_{CC} = 2.5\text{ V} \pm 10\%$, $\text{GND} = 0\text{ V}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
X_{TALK}	Crosstalk	$R_L = 50$, $f = 250\text{ MHz}$	-39	dB
O_{IRR}	OFF isolation	$R_L = 50$, $f = 250\text{ MHz}$	-40	dB
BW	Bandwidth (3 dB)	$R_L = 50$	0.9	GHz

SWITCHING CHARACTERISTICS

over operating range, $T_A = -40^{\circ}\text{C}$ to 125°C , $V_{CC} = 3.3\text{ V} \pm 10\%$, $\text{GND} = 0\text{ V}$

PARAMETER		MIN	TYP ⁽¹⁾	MAX	UNIT
t_{pd}	Propagation delay ^{(2) (3)}		0.25		ns
t_{ON}	Line enable time	S to D, nD		30	ns
		$\overline{\text{OE}}$ to D, nD		17	
t_{OFF}	Line disable time	S to D, nD		12	ns
		$\overline{\text{OE}}$ to D, nD		10	
$t_{\text{SK(O)}}$	Output skew between center port to any other port ⁽²⁾		0.1	0.2	ns
$t_{\text{SK(P)}}$	Skew between opposite transitions of the same output ($t_{\text{PHL}} - t_{\text{PLH}}$) ⁽²⁾		0.1	0.2	ns

(1) For Max or Min conditions, use the appropriate value specified under Electrical Characteristics for the applicable device type.

(2) Specified by design

(3) The bus switch contributes no propagational delay other than the RC delay of the on resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25 ns for 10-pF load. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagational delay to the system. Propagational delay of the bus switch, when used in a system, is determined by the driving circuit on the driving side of the switch and its interactions with the load on the driven side.

SWITCHING CHARACTERISTICS

over operating range, $T_A = -40^{\circ}\text{C}$ to 125°C , $V_{CC} = 2.5\text{ V} \pm 10\%$, $\text{GND} = 0\text{ V}$

PARAMETER		MIN	TYP ⁽¹⁾	MAX	UNIT
t_{pd}	Propagation delay ^{(2) (3)}		0.25		ns
t_{ON}	Line enable time	S to D, nD		50	ns
		$\overline{\text{OE}}$ to D, nD		32	
t_{OFF}	Line disable time	S to D, nD		23	ns
		$\overline{\text{OE}}$ to D, nD		12	
$t_{\text{SK(O)}}$	Output skew between center port to any other port ⁽²⁾		0.1	0.2	ns
$t_{\text{SK(P)}}$	Skew between opposite transitions of the same output ($t_{\text{PHL}} - t_{\text{PLH}}$) ⁽²⁾		0.1	0.2	ns

(1) For Max or Min conditions, use the appropriate value specified under Electrical Characteristics for the applicable device type.

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APPLICATION INFORMATION

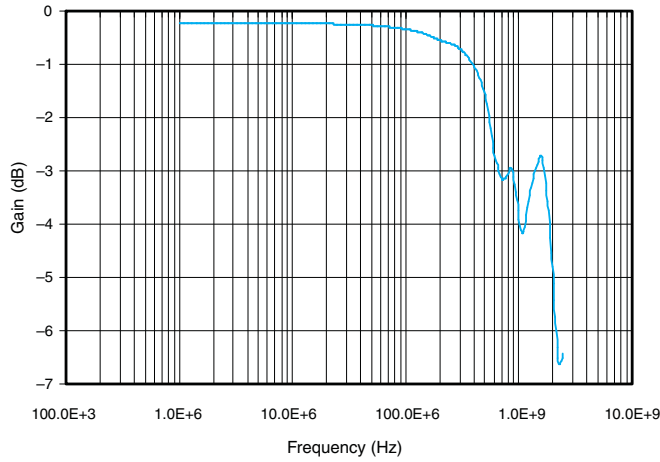


Figure 2. Gain vs Frequency

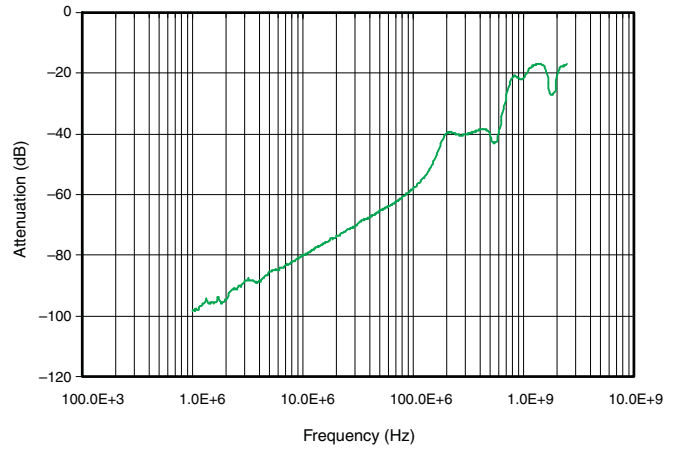


Figure 3. OFF Isolation vs Frequency

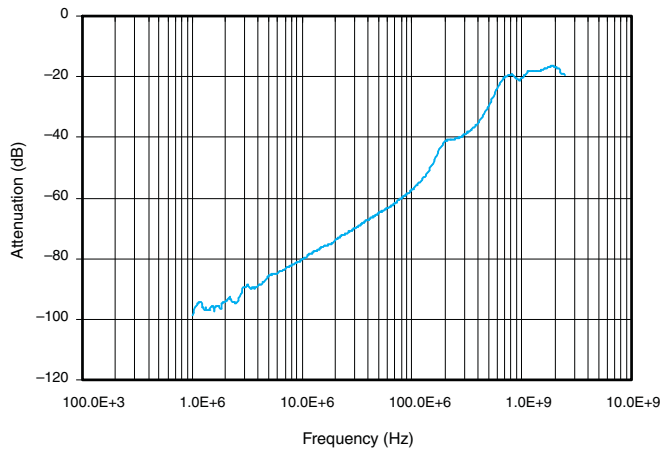


Figure 4. Crosstalk vs Frequency

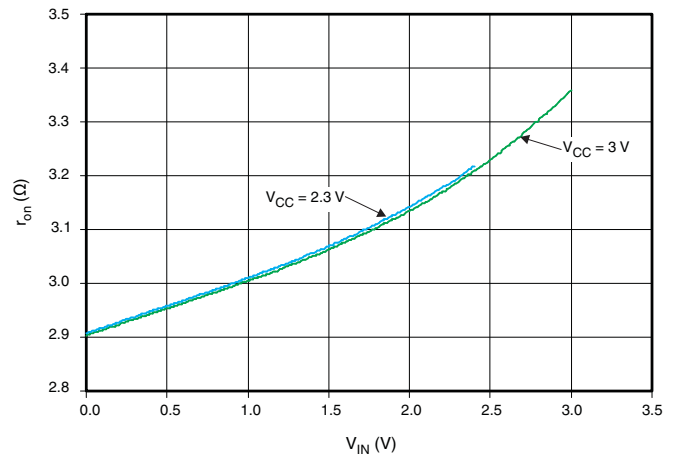


Figure 5. r_{on} vs V_{IN} ($I_{OUT} = -15$ mA)

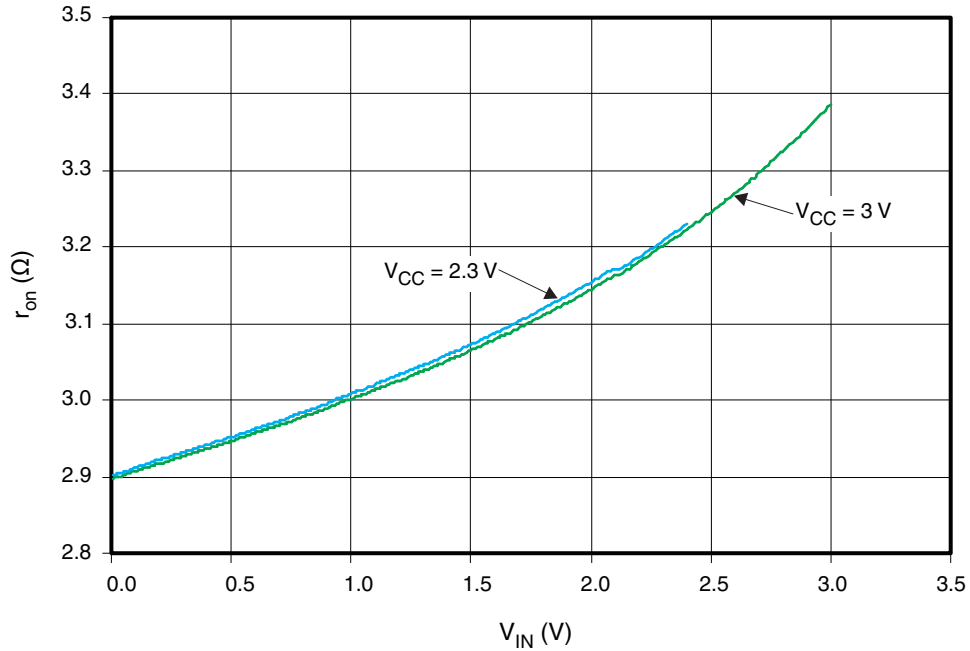


Figure 6. r_{ON} vs V_{IN} ($I_{OUT} = 30$ mA)

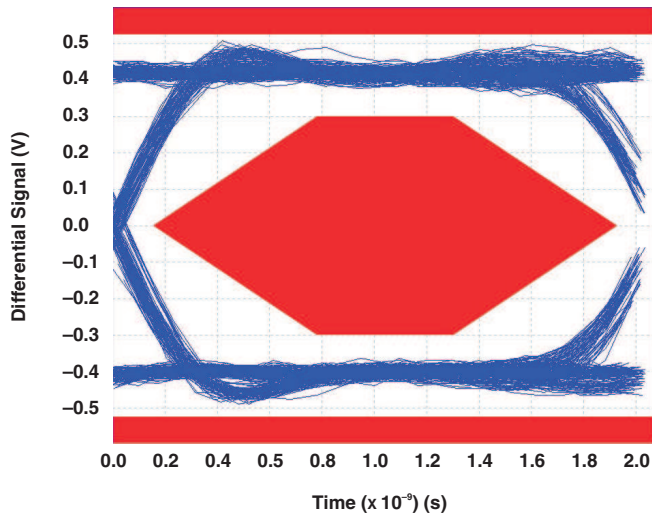


Figure 7. Eye Pattern: 480-Mbps USB Signal With No Switch (Through Path)

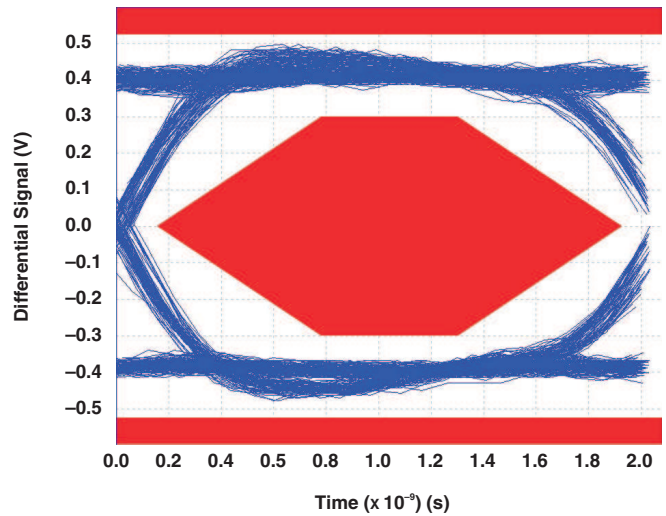


Figure 8. Eye Pattern: 480-Mbps USB Signal With Switch NC Path

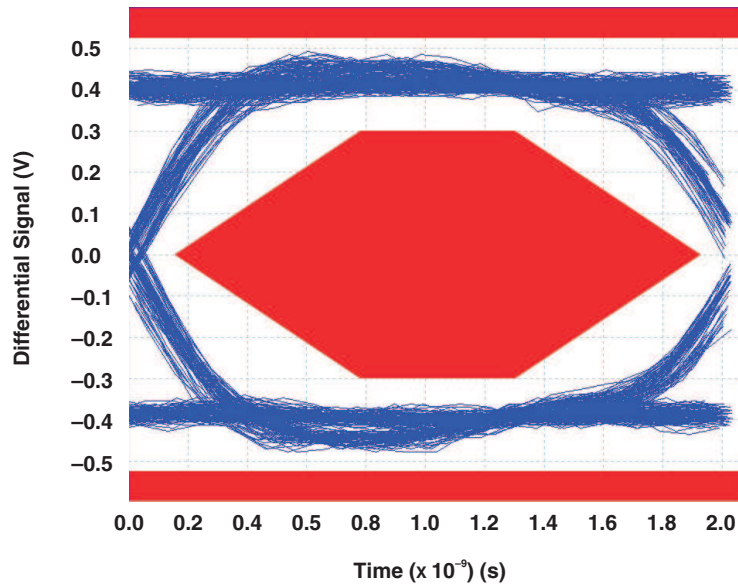
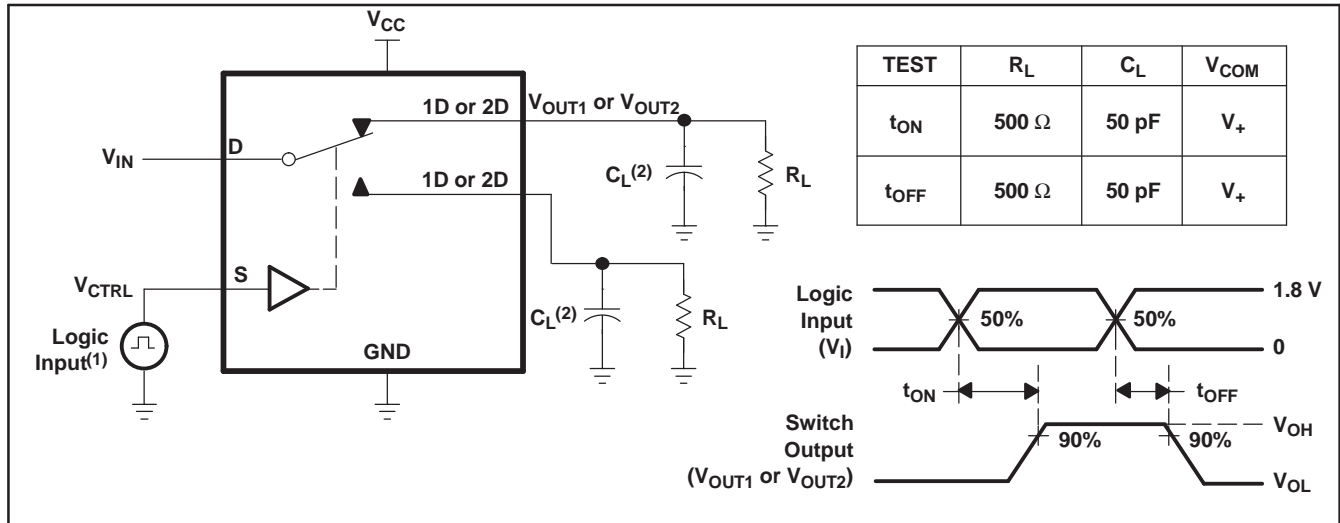


Figure 9. Eye Pattern: 480-Mbps USB Signal With Switch NO Path

PARAMETER MEASUREMENT INFORMATION



- (1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, ZO = 50 Ω, tr < 5 ns, tf < 5 ns.
- (2) CL includes probe and jig capacitance.

Figure 10. Turn-On (tON) and Turn-Off Time (tOFF)

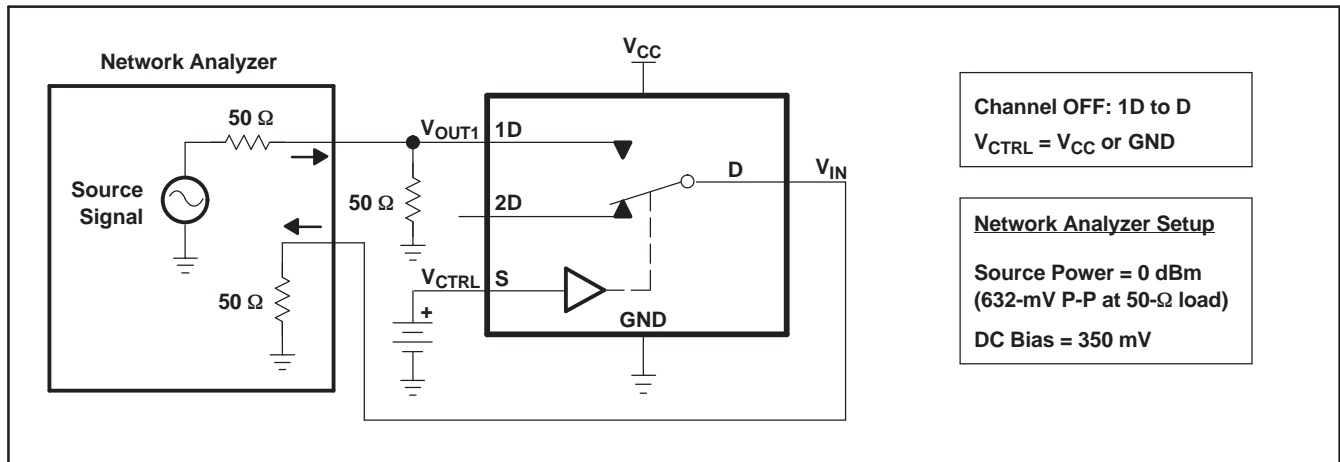


Figure 11. OFF Isolation (OISO)

PARAMETER MEASUREMENT INFORMATION (continued)

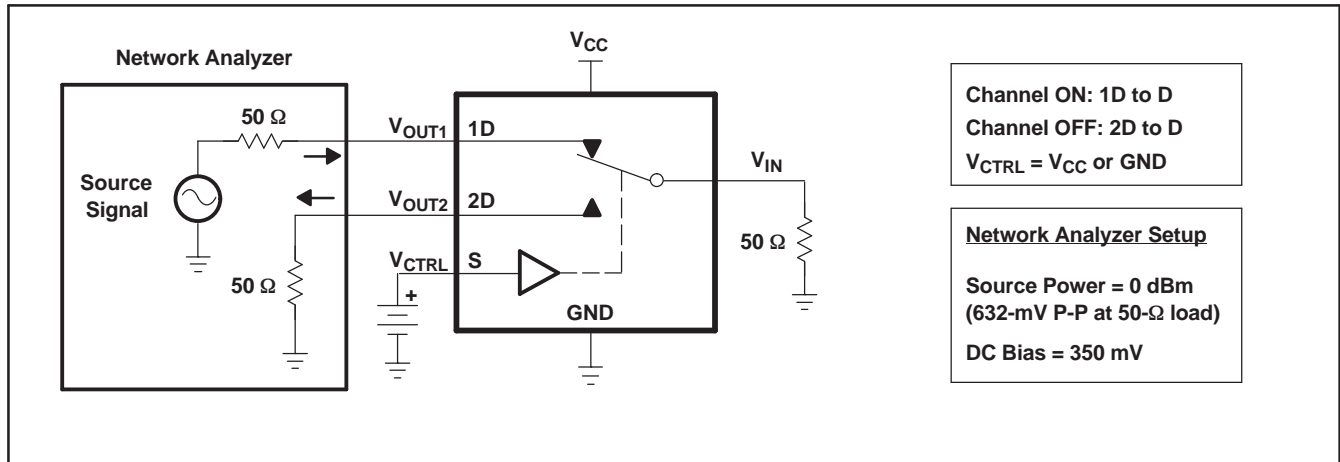


Figure 12. Crosstalk (X_{TALK})

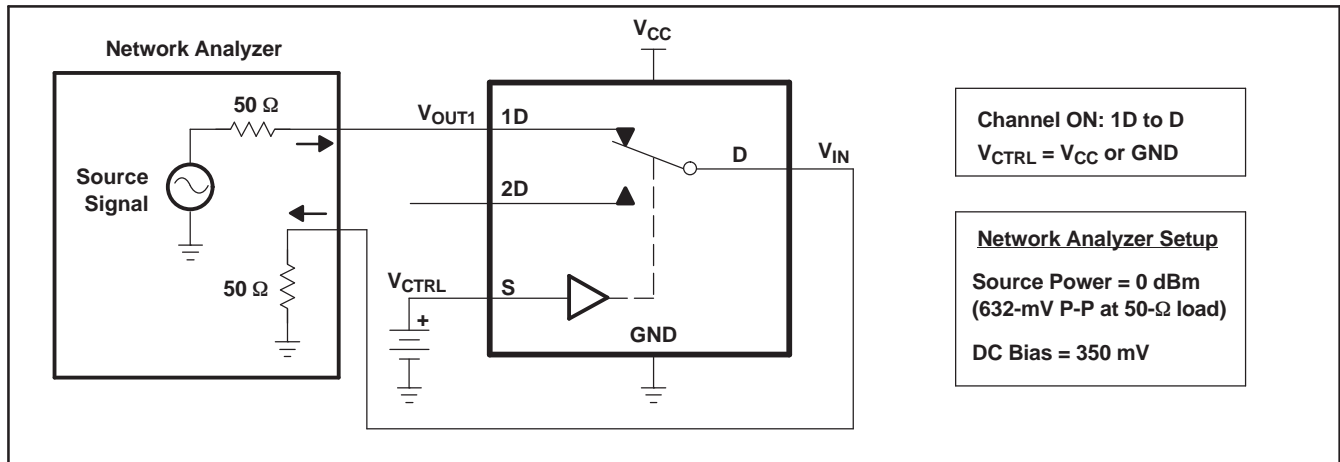


Figure 13. Bandwidth (BW)

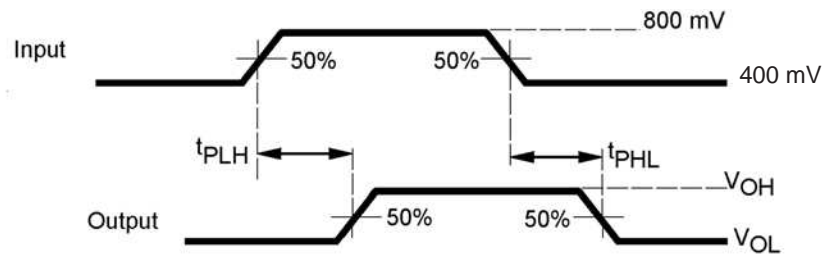


Figure 14. Propagation Delay

PARAMETER MEASUREMENT INFORMATION (continued)

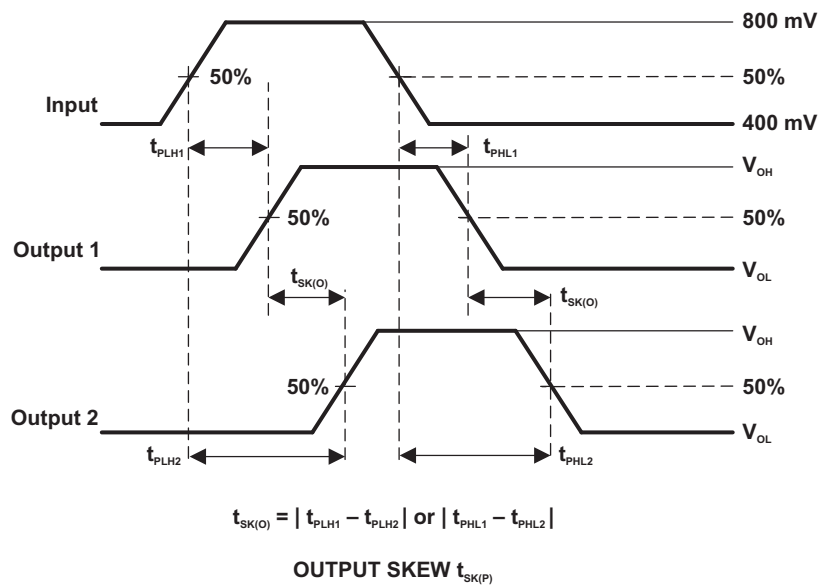
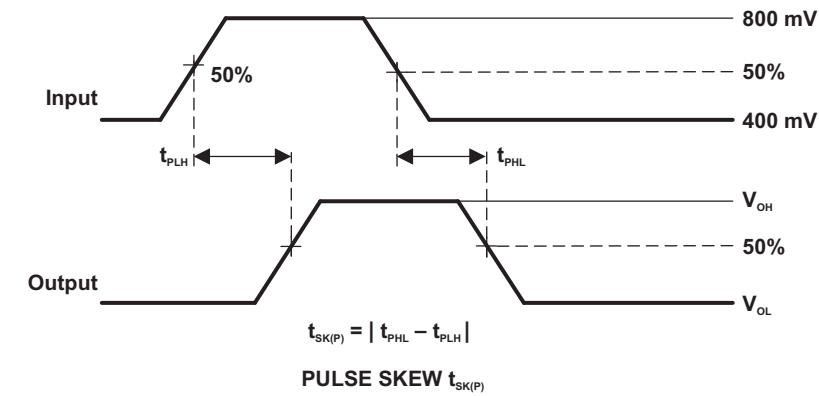


Figure 15. Skew Test

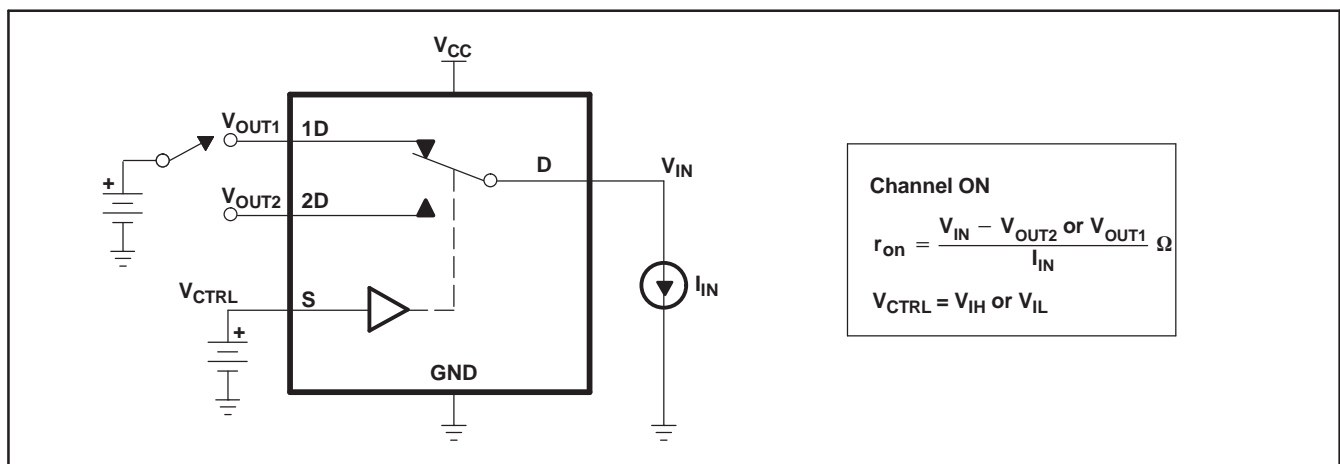


Figure 16. ON-State Resistance (r_{on})

PARAMETER MEASUREMENT INFORMATION (continued)

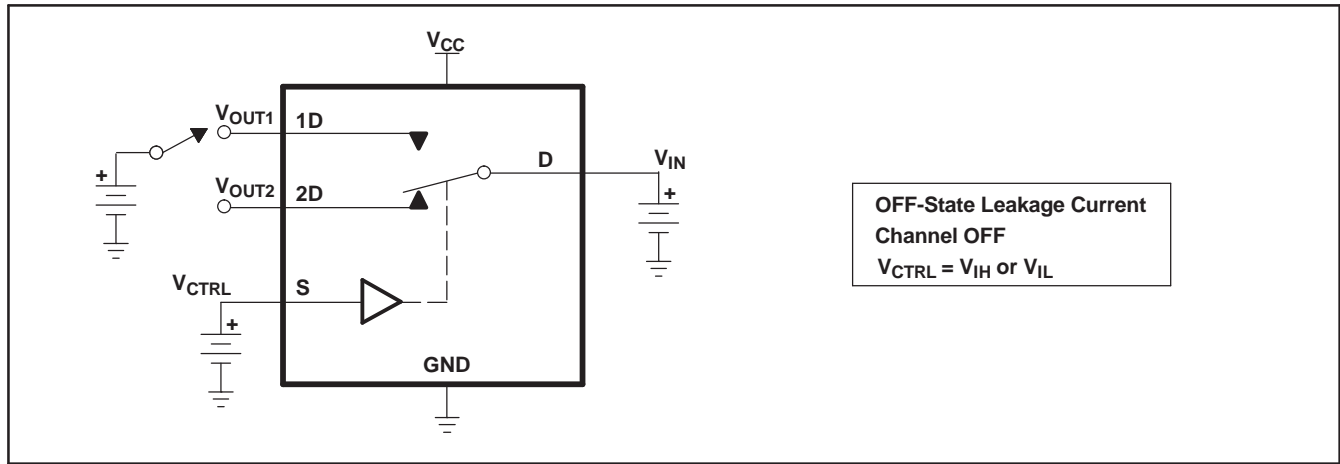


Figure 17. OFF-State Leakage Current

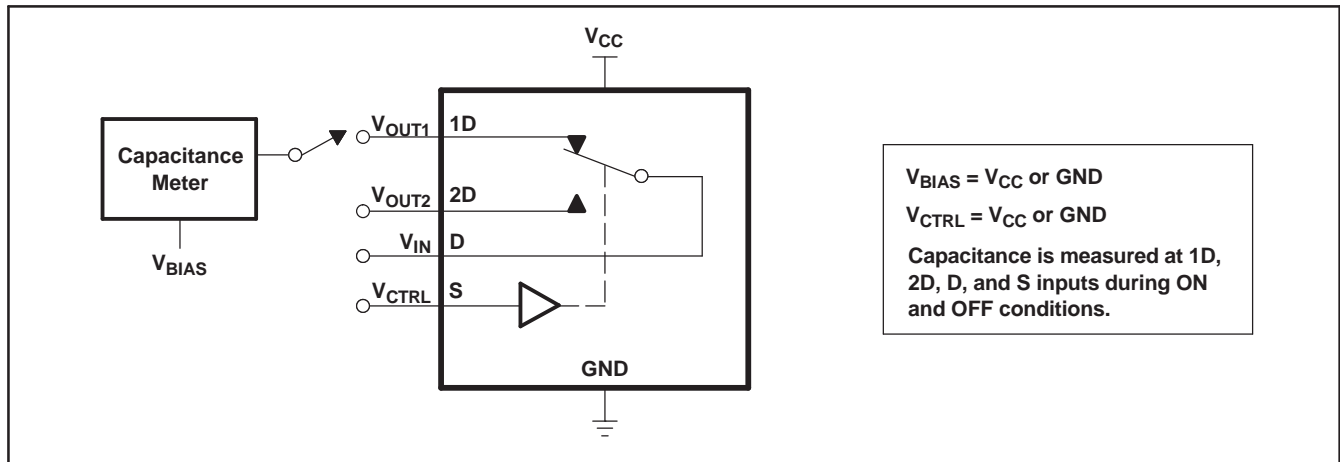


Figure 18. Capacitance

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
TS3USB221AQRSERQ1	ACTIVE	UQFN	RSE	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF TS3USB221A-Q1 :

- Catalog: [TS3USB221A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3USB221AQRSERQ1	UQFN	RSE	10	3000	180.0	8.4	1.68	2.13	0.76	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS

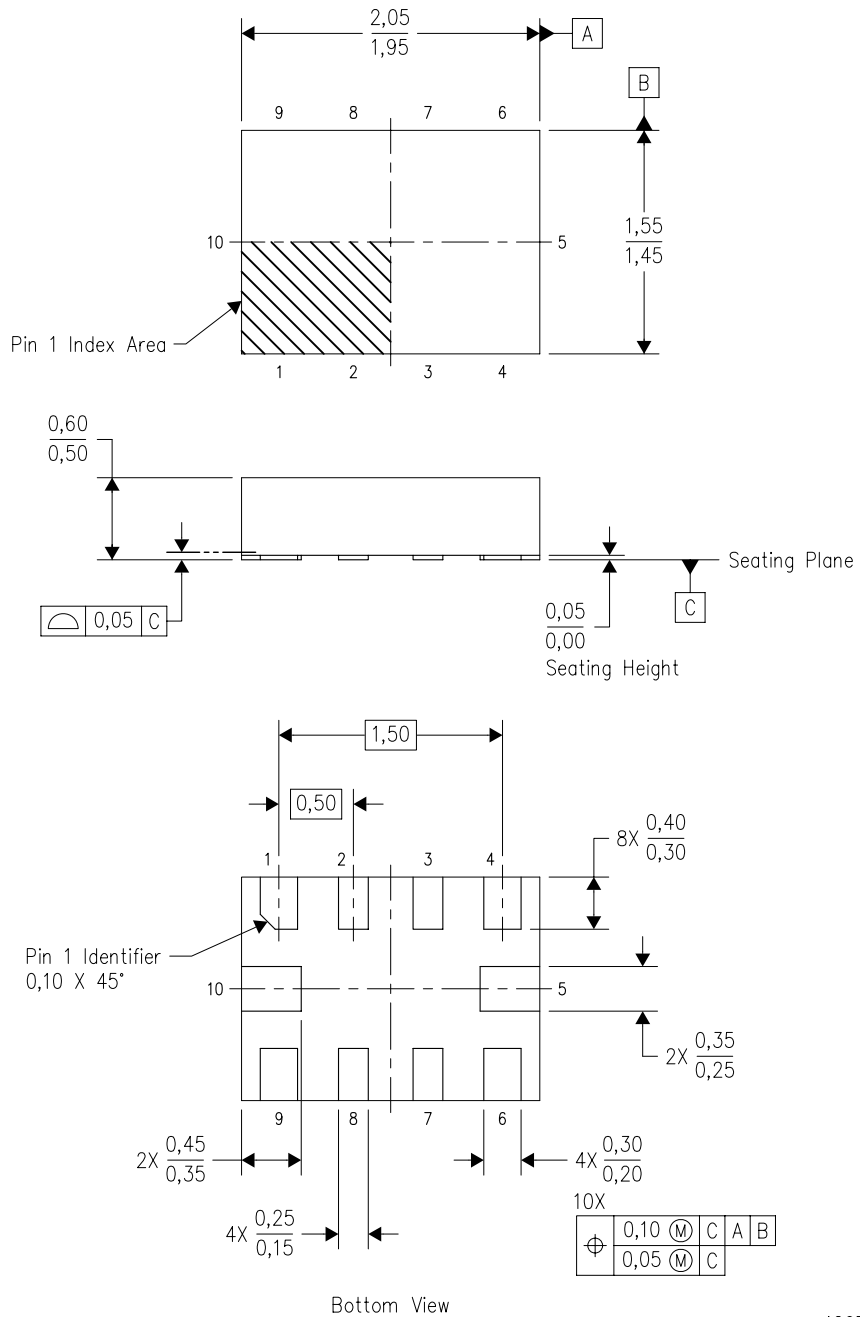


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3USB221AQRSERQ1	UQFN	RSE	10	3000	202.0	201.0	28.0

RSE (R-PUQFN-N10)

PLASTIC QUAD FLATPACK NO-LEAD

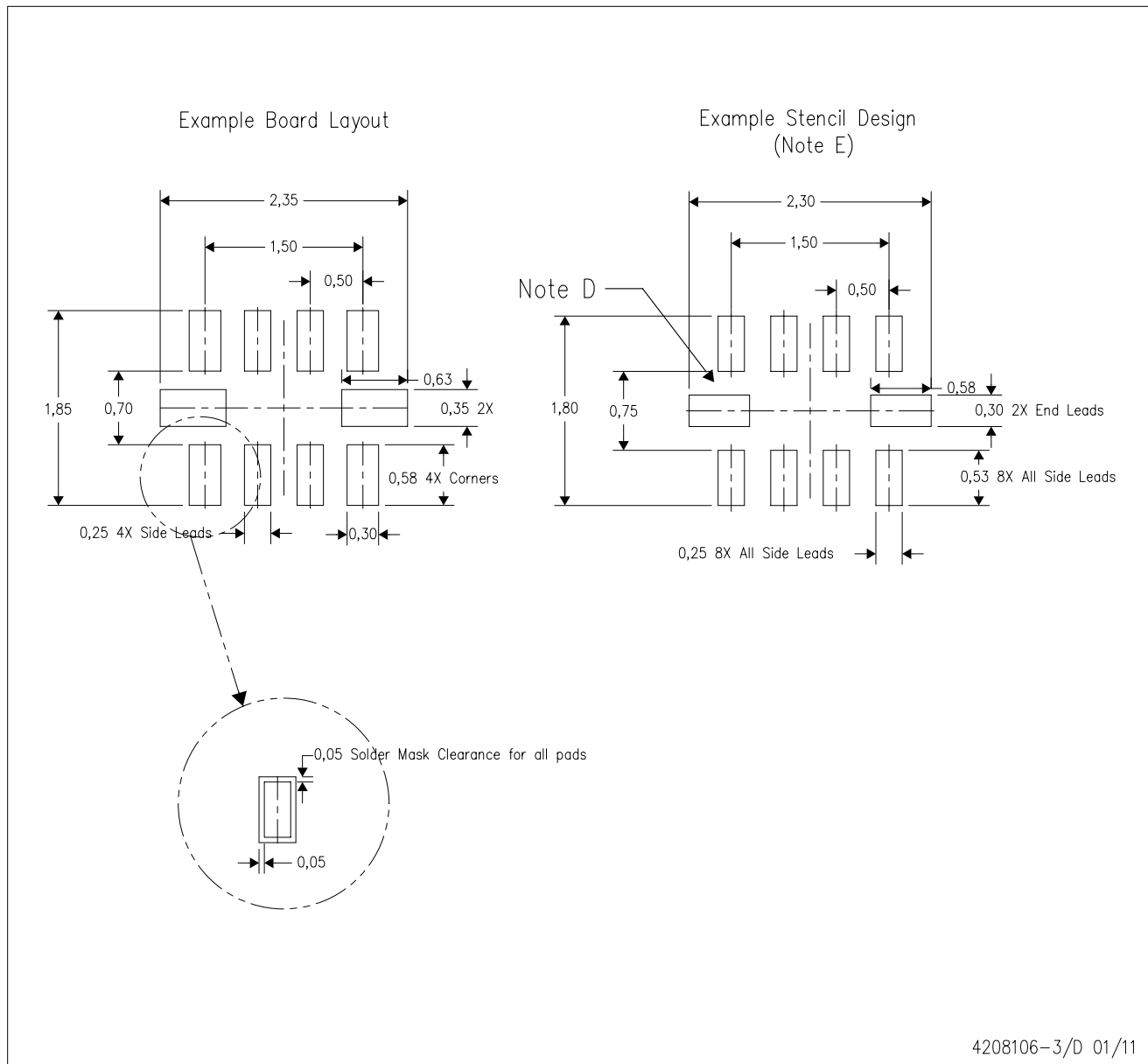


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- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) package configuration.
 - D. This package complies to JEDEC MO-288 variation UDFD.

RSE (R-PUQFN-N10)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
 - E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
 - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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